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IPC-6013A

Qualification and Performance Specification for Flexible Printed Boards

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with Amendment 1
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Amendment 1 - April 2000

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Developed by the Flexible Circuits Performance Specifications Subcommittee (D-12) of the Flexible Circuits Committee (D-10) of IPC

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Users of this publication are encouraged to participate in the development of future revisions.

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Acknowledgment

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1 SCOPE

This specification covers qualification and performance requirements of flexible printed wiring. The flexible printed wiring may be single-sided, double-sided, multilayer, or rigid-flex multilayer. All of these constructions may or may not include stiffeners, plated-through holes, and blind/buried vias.

1.1 Purpose The purpose of this specification is to provide requirements for qualification and performance of flexible printed wiring designed to IPC-2221 and IPC-2223.

1.2 Performance Classification, Wiring Type, and Installation Usage

1.2.1 Classification This specification recognizes that flexible printed wiring will be subject to variations in performance requirements based on end-use. These performance classes (Class 1, Class 2, and Class 3) are defined in IPC-6011.

1.2.2 Wiring Type Performance requirements are established for the different types of flexible printed wiring, classified as follows:

Type 1 Single-sided flexible printed wiring containing one conductive layer, with or without stiffeners.

Type 2 Double-sided flexible printed wiring containing two conductive layers with plated-through holes, with or without stiffeners.

Type 3 Multilayer flexible printed wiring containing three or more conductive layers with plated-through holes, with or without stiffeners.

Type 4 Multilayer rigid and flexible material combinations containing three or more conductive layers with plated-through holes.

Type 5 Flexible or rigid-flex printed wiring containing two or more conductive layers without plated-through holes.

1.2.3 Installation Uses

Use A Capable of withstanding flex during installation.

Use B Capable of withstanding continuous flexing for the number of cycles as specified on the procurement documentation.

Use C High temperature environment (over 105 °C [221 °F]).

Use D UL Recognition.

1.2.4 Selection for Procurement For procurement purposes, performance class and installation usage **shall** be specified in the procurement documentation.

The documentation **shall** provide sufficient information to the supplier so that the supplier can fabricate the flexible printed wiring and ensure that the user receives the desired product. Information that should be included in the procurement documentation is shown in IPC-D-325.

1.2.4.1 Selection (Default) The procurement documentation should specify the requirements that can be selected within this specification. However, in the event that these selections are not made in the documentation, the following default selections **shall** apply:

Performance Class – Class 2
Installation Usage – Use A

1.2.5 Material, Plating Process and Final Finish

1.2.5.1 Laminate Material Laminate material is identified by numbers and/or letters, classes and types as specified by the appropriate specification listed in the procurement documentation.

1.2.5.2 Plating Process The copper plating process used to provide the main conductor in the holes is identified by a single number as follows:

1. Acid copper electroplating only.
2. Pyrophosphate copper electroplating only.
3. Acid and/or pyrophosphate copper electroplating.
4. Additive/electroless copper.

1.2.5.3 Final Finish The final finish can be but is not limited to one of the designators given below or a combination of several platings and is dependent on assembly processes and end-use. The procurement documentation **shall** specify finish designators. Unless otherwise specified, thicknesses given in Table 1-1 **shall** apply.

S Solder Coating (Table 1-1)

T Electrodeposited Tin-Lead (fused) (Table 1-1)

X Either Type S or T (Table 1-1)

TLU Electrodeposited Tin-Lead (unfused) (Table 1-1)

G Gold Electroplate for Edge Board Connectors (Table 1-1)

GS Gold Electroplate for Areas to be Soldered (Table 1-1)

GWB-1 Gold Electroplate for areas to be wire bonded (ultrasonic)

GWB-2 Gold Electroplate for areas to be wire bonded (thermosonic)

N Nickel Electroplate for Edge Board Connectors (Table 1-1)

NB Nickel Electroplate as a Barrier to Copper-Tin Diffusion (Table 1-1)

OSP Organic Solderability Preservative (tarnish and solderability protection during storage and assembly processes) (Table 1-1)

ENIG Electroless Nickel Immersion Gold

IS Immersion Silver

IT Immersion Tin

C Bare Copper (Table 1-1)

Y Other

1.3 Interpretation ''**Shall**,'' the imperative form of the verb, is used throughout this standard whenever a requirement is intended to express a provision that is mandatory. Deviation from a ''**shall**'' requirement may be considered if sufficient data is supplied to justify the exception.

The words ''should'' and ''may'' are used whenever it is necessary to express nonmandatory provisions.

''Will'' is used to express a declaration of purpose. To assist the reader, the word ''**shall**'' is presented in bold characters.

2 APPLICABLE DOCUMENTS

The following specifications form a part of this specification to the extent specified herein. If a conflict of requirements exists between IPC-6013 and the listed applicable documents, IPC-6013 **shall** take precedence.

2.1 IPC[1]

IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits

IPC-DD-135 Qualification for Deposited Organic Interlayer Dielectric Materials for Multichip Modules

IPC-CF-148 Resin Coated Metal for Printed Boards

IPC-D-325 Documentation Requirements for Printed Wiring

IPC-A-600 Acceptability of Printed Boards

IPC-TM-650 Test Methods Manual[2]

2.1.1 Microsectioning

2.1.1.2 Microsectioning-Semi or Automatic Technique Microsection Equipment (Alternate)

2.3.15 Purity, Copper Foil or Plating

2.3.38 Surface Organic Contaminant Detection List

2.3.39 Surface Organic Contaminant Identification Test (Infrared Analytical Method)

2.4.1 Adhesion, Tape Testing

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2.4.3.1 Flexural Fatigue and Ductility, Flexible Printed Wiring

2.4.18.1 Tensile Strength and Elongation, In-House Plating

2.4.20 Terminal Bond Strength, Flexible Printed Wiring

2.4.22 Bow and Twist

2.4.28.1 Adhesion, Solder Resist (Mask) Tape Test Method

2.4.36 Rework Simulation, Plated-Through Holes for Leaded Components

2.4.41.2 Coefficient of Thermal Expansion - Strain Gage Method

2.5.7 Dielectric Withstand Voltage, PWB

2.6.1 Fungus Resistance Printed Wiring Materials

2.6.3 Moisture and Insulation Resistance, Printed Boards

2.6.4 Outgassing, Printed Boards

2.6.7.2 Thermal Shock and Continuity, Printed Boards

2.6.8 Thermal Stress, Plated-Through Holes

IPC-QL-653 Qualification of Facilities that Inspect/Test Printed Boards, Components and Materials

IPC-SM-840 Qualification and Performance of Permanent Solder Mask

IPC-2221 Generic Standard on Printed Board Design

IPC-2223 Sectional Design Standard for Flexible Printed Boards

IPC-2251 Design Guide for the Packaging of High Speed Electronic Circuits

IPC-4101 Specification for Base Materials for Rigid and Multilayer Printed Boards

1. www.ipc.org
2. Current and revised IPC Test Methods are available through IPC-TM-650 subscription and on the IPC Web site (www.ipc.org/html/testmethods.htm).

Table 1-1 Final Finish, Surface Plating and Coating Thickness Requirements

Code	Finish	Class 1	Class 2	Class 3
		Final Finish		
S	**Solder Coating** over Bare Copper	Coverage and Solderable[5]	Coverage and Solderable[5]	Coverage and Solderable[5]
T	**Electrodeposited Tin-Lead** (Fused) (min.)	Coverage and Solderable[5]	Coverage and Solderable[5]	Coverage and Solderable[5]
X	Either Type S or T	As indicated by code		
TLU	**Electrodeposited Tin-Lead Unfused** (min.)	8.0 µm [315 µin]	8.0 µm [315 µin]	8.0 µm [315 µin]
G	**Gold Electroplate** (min.) for flexible printed wiring edge connectors and areas not intended to be soldered	0.8 µm [31.5 µin]	0.8 µm [31.5 µin]	1.3 µm [51.2 µin]
GS	**Gold Electroplate** (max.) for areas intending to be soldered	0.8 µm [31.5 µin]	0.8 µm [31.5 µin]	0.8 µm [31.5 µin]
GWB-1	**Gold Electroplate** for areas to be wire bonded (ultrasonic) (min.)	0.05 µm [1.97 µin]	0.05 µm [1.97 µin]	0.05 µm [5.91 µin]
GWB-2	**Gold Electroplate** for areas to be wire bonded (thermosonic) (min.)	0.3 µm [11.8 µin]	0.3 µm [11.8 µin]	0.8 µm [31.5 µin]
N	**Nickel - Electroplate** for Edge Board Connectors (min.)	2.0 µm [78.7 µin]	2.5 µm [98.4 µin]	2.5 µm [98.4 µin]
NB	**Nickel - Electroplate** as a Barrier to Copper-Tin Diffusion[1] (min.)	1.0 µm [39.4 µin]	1.3 µm [51.2 µin]	1.3 µm [51.2 µin]
OSP	**Organic Solderability Preservative**	Solderable	Solderable	Solderable
ENIG	**Electroless Nickel Immersion Gold**	3 µm [118 µin] (min.)	3 µm [118 µin] (min.)	3 µm [118 µin] (min.)
	Immersion Gold	0.05 µm [1.97 µin] (min.)	0.05 µm [1.97 µin] (min.)	0.05 µm [1.97 µin] (min.)
IS	**Immersion Silver**	Solderable	Solderable	Solderable
IT	**Immersion Tin**	Solderable	Solderable	Solderable
C	**Bare Copper**	As indicated in Table 3-10 and/or Table 3-11		
		Surface and Hole Plating		
Copper[2] (min. average)		**Holes**		
	Type 2	12 µm [472 µin]	12 µm [472 µin]	12 µm [472 µin]
	Type 3, 4 ≤6 layers	25 µm [984 µin]	25 µm [984 µin]	25 µm [984 µin]
	Type 3, 4 >6 layers	35 µm [1,378 µin]	35 µm [1,378 µin]	35 µm [1,378 µin]
	Copper Min. Thin Areas[3]			
	Type 2	10 µm [394 µin]	10 µm [394 µin]	10 µm [394 µin]
	Type 3, 4 ≤6 layers	20 µm [787 µin]	20 µm [787 µin]	20 µm [787 µin]
	Type 3, 4 >6 layers	30 µm [1,181 µin]	30 µm [1,181 µin]	30 µm [1,181 µin]
Copper Type[4]		**Blind Vias[4]**		
	(min. average)	20 µm [787 µin]	20 µm [787 µin]	25 µm [984 µin]
	(min. at thin area)	18 µm [709 µin]	18 µm [709 µin]	20 µm [787 µin]
Copper Type[4]		**Buried Vias**		
	(min. average)	13 µm [512 µin]	15 µm [592 µin]	15 µm [592 µin]
	(min. at thin area)	11 µm [433 µin]	13 µm [512 µin]	13 µm [512 µin]

[1] Nickel plating used under the tin-lead or solder coating for high temperature operating environments act as a barrier to prevent the formation of copper-tin compounds.

[2] Copper plating (1.2.5.2) thickness applies to surface and hole walls.

[3] For Class 3 boards having a drilled hole diameter <0.35 mm [0.0138 in] and having an aspect ratio >3.5:1, the minimum thin area copper plating in the hole **shall** be 25 µm [984 µin].

[4] Low Aspect Ratio Blind Vias refer to blind vias produced using a controlled depth mechanism (e.g., laser, mechanical, plasma or photo defined). All performance characteristics for plated holes, as defined in this document, **shall** be met.

[5] See also 3.3.5.

IPC-4202 Flexible Bare Dielectrics for use in Flexible Printed Wiring

IPC-4203 Adhesive Coated Dielectrics Films for Use in Fabrication of Flexible Printed Wiring

IPC-4204 Metal-Clad Flexible Dielectrics for Use in Fabrication of Flexible Printed Wiring

IPC-4552 Electroless Nickel/Immersion Gold Plating for Electronic Interconnections

IPC-4562 Copper Foil for Printed Wiring Applications

IPC-6011 Generic Performance Specification for Printed Boards

IPC-7711 Rework of Electronic Assemblies

IPC-9252 Guidelines and Requirements for Electrical Testing of Unpopulated Printed Boards

2.2 Joint Industry Standards[3]

J-STD-003 Solderability Tests for Printed Boards

J-STD-006 Requirements for Electronic Grade Solder Alloys and Fluxed and Non-Fluxed Solid Solders for Electronic Soldering Applications

2.3 Federal[4]

SAE-AMS-QQ-N-290 Nickel Plating (Electrodeposited)

2.4 American Society for Testing and Materials[5]

ASTM B 488 Standard Specification for Electrodeposited Coatings of Gold for Engineering Uses

ASTM B 579 Standard Specification for Electrodeposited Coatings of Tin-Lead Alloy

2.5 National Electrical Manufacturers Association[6]

NEMA LI-1 Industrial Laminate Thermosetting Product

2.6 American Society for Quality[7]

H0862 Zero Acceptance Number Sampling Plans

3 REQUIREMENTS

Flexible printed wiring furnished under this specification **shall** meet or exceed all of the requirements of the specific performance class as required by the procurement documentation. Although conformance to the detailed requirements may be determined by examination of specific quality control coupons, these requirements apply to all coupons or sample flexible printed wiring and to deliverable flexible printed wiring. These requirements are also based on the assumption that the flexible printed wiring was designed to the appropriate design standard.

3.1 Terms and Definitions

3.1.1 Coverlayer An outer layer of insulating material applied over the conductive pattern on the surface of the printed board with openings or apertures providing access to selected locations.

3.1.2 Coverfilm A film of dielectric material with adhesive used for the coverlayer, usually identical with the base layer, which is bonded over the etched conductor run to insulate them.

3.1.3 Covercoat A layer of dielectric applied as a liquid or photo-definable film over an imaged conductor pattern.

3.2 Material All materials used in construction of the flexible printed wiring **shall** comply with applicable specifications and the procurement documentation. The user has the responsibility to specify on the procurement documentation materials capable of meeting the requirements of this specification and end item use.

Note: When possible, material call-out information should be reviewed with the supplier so as to obtain concurrence that the part will meet the requirements of this specification and, if necessary, to update the procurement documentation accordingly.

3.2.1 Flexible Material Options At the supplier's option, flexible metal-clad dielectrics and adhesive coated dielectric films may be manufactured using individual components per IPC-4562, IPC-4202, and IPC-4203. In addition, materials per IPC-4204 may be substituted where individual components are specified.

3.2.2 Laminates and Bonding Material for Multilayer Flexible Printed Wiring Metal-clad laminates, unclad laminates, and bonding material (prepreg) should be selected using IPC-4101, IPC-4202, IPC-4203, IPC-4204, or NEMA LI 1-1989. The specification sheet number, metal cladding type and metal clad thickness (weight) should be as specified in the procurement documentation. When there are specific requirements, it is necessary to specify those requirements on the material procurement documentation.

3. www.ipc.org
4. www.sae.org
5. www.astm.org
6. www.nema.org
7. www.asq.org

3.2.3 External Bonding Materials The material used to adhere external heat sinks or stiffeners to the flexible printed wiring should be selected from IPC-4202, IPC-4203, IPC-4204, or as specified on the procurement documentation.

3.2.4 Other Dielectric Materials Photoimageable dielectrics should be selected from IPC-DD-135 and specified on the procurement documentation. Other dielectric materials may be specified on the procurement documentation.

3.2.5 Metal Foils Copper foil should be in accordance with IPC-4562. Foil type, foil grade, foil thickness, bond enhancement treatment, and foil profile should be specified on the master drawing if critical to the function of the flexible printed wiring. Resin coated copper foil should be in accordance with IPC-CF-148. Resistive metal foil should be in accordance with the applicable specification and the procurement documentation.

3.2.6 Metallic Platings and Coatings Thickness of the platings/coatings in 3.2.6.1 through 3.2.6.8 **shall** be in accordance with Table 1-1. Thickness values are excluded for coating (S) solder coating and/or coating (T) fused electrodeposited tin-lead plating. Coating S and T require visual coverage and acceptable solderability testing per J-STD-003. Coverage of platings and metallic coatings does not apply to vertical conductor edges; conductor surfaces may have exposed copper in areas not to be soldered within the limits of 3.5.3.6. Selective plating and coatings **shall** be confined to the areas defined on the procurement documentation.

Note: The category of solderability testing **shall** be specified by the supplier per J-STD-003; however, in the event it is not specified, the supplier **shall** test to Category 2 (steam aging is not required).

3.2.6.1 Electroless Depositions and Coatings Electroless depositions and coatings **shall** be sufficient for subsequent plating processes and may be either electroless plated metal, vacuum deposited metal, or metallic or nonmetallic conductive coatings.

3.2.6.2 Electrodeposited Copper When specified, electrodeposited copper platings **shall** meet the following criteria. Frequency of testing **shall** be determined by the manufacturer to ensure process control.

a) When tested as specified in IPC-TM-650, Method 2.3.15, the purity of copper **shall** be no less than 99.50%.

b) When tested as specified in IPC-TM-650, Method 2.4.18.1, with the exception of removing the bake step in section 5 within the test method, using 50 µm - 100 µm [1969 µin - 3937 µin] thick samples, the tensile strength **shall** be no less than 36,000 PSI [248 MPa] and the elongation **shall** be no less than 12%.

c) The ductility **shall** not be less than 30% when tested in accordance with IPC-TM-650, Method 2.4.2.1.

3.2.6.3 Additive Copper Depositions Additive/electroless copper platings applied as the main conductor metal **shall** meet the requirements of this specification.

3.2.6.4 Tin-Lead Electrodeposited Tin-Lead plating **shall** meet the composition (50% to 70% tin) requirements of ASTM B-579. Fusing is required unless the unfused option is selected, wherein the thickness specified in Table 1-1 applies.

3.2.6.5 Solder Coating The solder used for solder coating **shall** be Sn60A, Sn60C, Pb40A, Pb36A, Pb36B, Pb36C, Sn63A, Sn63C, or Pb37A, per J-STD-006.

3.2.6.6 Nickel Electrodeposited Nickel plating **shall** be in accordance with SAE AMS QQ-N-290, Class II.

3.2.6.7 Electrodeposited Gold Plating Electrodeposited gold plating **shall** be in accordance with ASTM B 488. Purity, hardness and thickness **shall** be as specified on the procurement documentation. Gold plating thickness on areas to be wire bonded **shall** be as specified on the procurement documentation.

3.2.6.8 Electroless Nickel Immersion Gold Plating Electroless nickel immersion gold plating **shall** be in accordance with IPC-4552.

3.2.6.9 Other Metals and Coatings Other depositions, such as electroless nickel, immersion gold, immersion silver, palladium, rhodium, tin, solder alloys, etc., may be used, provided they are specified on the procurement documentation.

3.2.7 Organic Solderability Protective Coatings (OSP) OSPs are anti-tarnish and solderability protectors applied to copper to withstand storage and assembly processes in order to maintain solderability of surfaces. The coating storage, pre-assembly baking and sequential soldering processes impact solderability. The specific solderability retention requirement, if applicable, **shall** be specified in the procurement documentation.

3.2.8 Solder Resist When permanent solder resist coating is specified, it **shall** be a polymer coating conforming to IPC-SM-840.

3.2.9 Fusing Fluids and Fluxes The composition of the fusing fluids and fluxes used in solder coating applications **shall** be capable of cleaning and fusing the electrodeposited tin-lead plating and bare copper to allow for a smooth

adherent coating. The fusing fluid **shall** act as a heat transfer and distribution medium to prevent damage to the bare laminate of the flexible printed wiring. The type and composition of the fusing fluid **shall** be optional to the flexible printed wiring manufacturer.

3.2.10 Marking Inks Marking inks **shall** be permanent, nonnutrient (fungistatic) polymer inks and **shall** be specified in the procurement documentation. Marking inks **shall** be applied to either the flexible printed wiring or to a label applied to the flexible printed wiring. Marking inks and labels must be capable of withstanding fluxes, cleaning solvents, soldering, and cleaning and coating processes encountered in later manufacturing processes. If a conductive marking ink is used, the marking **shall** be treated as a conductive element on the flexible printed wiring.

3.2.11 Hole Fill Insulation Material Electrical insulation material used for hole fill for metal core flexible printed wiring **shall** be as specified on the procurement documentation.

3.2.12 Heatsink Planes, External Thickness and materials for construction of heatsink planes and insulation material **shall** be as specified in the procurement documentation.

3.3 Visual Examination Finished flexible printed wiring **shall** be examined in accordance with the following procedure. They **shall** be of uniform quality and **shall** conform to 3.3.1 through 3.3.9.

Visual examination for applicable attributes **shall** be conducted at 3 diopters (approx.1.75X). If the acceptable condition of a suspected defect is not apparent, it should be verified at progressively higher magnifications (up to 40X) to confirm that it is a defect. Dimensional requirements such as spacing or conductor width measurements may require other magnifications and devices with reticles or scales in the instrument, which allow accurate measurements of the specified dimensions. Contract or specification may require other magnifications.

3.3.1 Profile

3.3.1.1 Edges, Rigid Section Nicks, crazing or haloing along the edges of the flexible printed wiring, cutouts, and nonplated-through holes are acceptable, provided the penetration does not exceed 50% of the distance from the edge to the nearest conductor or 2.5 mm [0.0984 in], whichever is less. Edges **shall** be clean cut and without metallic burrs. Nonmetallic burrs are acceptable as long as they are not loose and/or do not affect fit and function. Panels that are scored or routed with a breakaway tab **shall** meet the depanelization requirements of the assembled flexible printed wiring.

3.3.1.2 Edges, Flexible Section The trimmed edges of the flexible printed wiring or the flexible section of finished rigid-flex printed wiring **shall** be free of burrs, nicks, or delamination in excess of that allowed in the procurement documentation. Tears **shall not** be allowed in Type 1 or Type 2 flexible printed wiring. When nicks and tears occur as a result of tie-in tabs to facilitate circuit removal, the extent of these imperfections **shall** be agreed upon between user and supplier. Minimum edge to conductor spacing **shall** be specified in the procurement documentation.

3.3.1.3 Transition Zone, Rigid Area to Flexible Area The transition zone is the area centered on the edge of the rigid portion from which the flex portion extends. The inspection range is limited to 3 mm [0.118 in], centered on the transition, which is the edge of the rigid portion (see Figure 3-1). Visual imperfections inherent to the fabrication technique (i.e., adhesive squeeze-out, localized deformation of dielectric and conductors, protruding dielectric materials, crazing, or haloing) **shall not** be cause for rejection. Imperfections in excess of that allowed **shall** be agreed upon between the fabricator and user, or as so stated on the procurement documentation.

3.3.2 Construction Imperfections - Rigid Laminate imperfections include those characteristics that are both internal and external within the printed board but are visible from the surface.

3.3.2.1 Measling Measling is acceptable for all classes of end product, with the exception of high-voltage applications. Refer to IPC-A-600 for more information.

3.3.2.2 Crazing Crazing is acceptable for all classes of end product provided the imperfection does not reduce the conductor spacing below the minimum and there is no propagation of the imperfection as a result of thermal testing that replicates the manufacturing process. For Class 2 and 3, the distance of crazing **shall not** span more than 50% of the distance between adjacent conductors.

3.3.2.3 Delamination/Blister Delamination and blistering is acceptable for all classes of end product provided the area affected by imperfections does not exceed 1% of the board area on each side and does not reduce the spacing between conductive patterns below the minimum conductor spacing. There **shall** be no propagation of imperfections as a result of thermal testing that replicates the manufacturing process. For Class 2 and 3, the blister or delamination **shall not** span more than 25% of the distance between adjacent conductive patterns.

3.3.2.4 Foreign Inclusions Translucent particles trapped within the board **shall** be acceptable. Other particles trapped within the board **shall** be acceptable, provided the

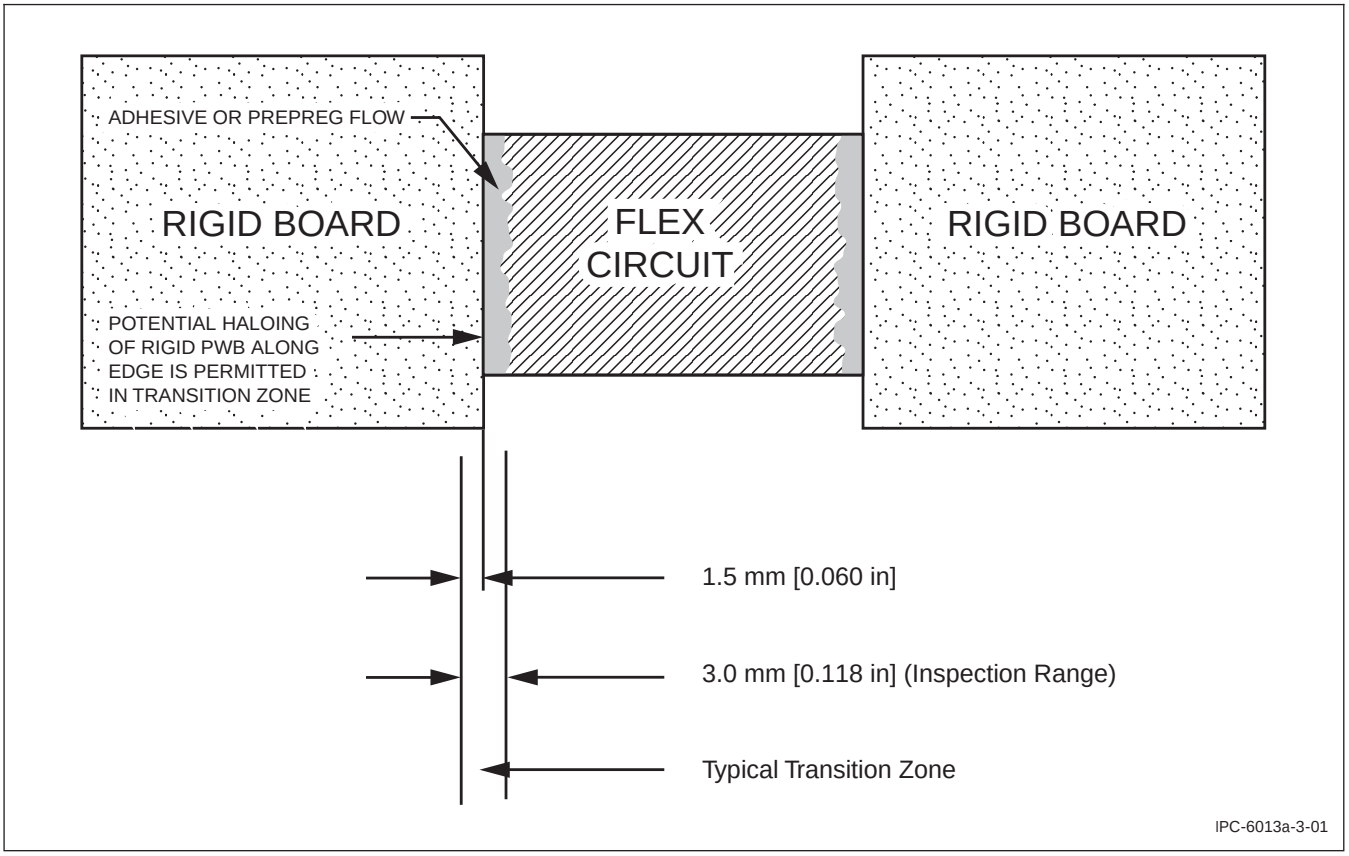

Figure 3-1 Transition Zone

particle does not reduce the spacing between adjacent conductors to below the minimum spacing specified in 3.5.2.

3.3.2.5 Weave Exposure Weave exposure or exposed/disrupted fibers are acceptable for all Classes provided the imperfection does not reduce the remaining conductor spacing (excluding the area(s) with weave exposure) below the minimum. Refer to IPC-A-600 for more information.

3.3.2.6 Scratches, Dents, and Tool Marks Scratches, dents, and tool marks are acceptable, provided they do not bridge conductors or expose/disrupt fibers greater than allowed in 3.3.2.4 and 3.3.2.5 and do not reduce the dielectric spacing below the minimum specified.

3.3.2.7 Surface Microvoids Surface microvoids are acceptable, provided they do not exceed 0.8 mm [0.0315 in] in the longest dimension, bridge conductors, or exceed 5% of the total flexible printed wiring area.

3.3.2.8 Color Variations in Bond Enhancement Treatment Mottled appearance or color variation in bond enhancement treatment is acceptable. Random missing areas of treatment **shall not** exceed 10% of the total conductor surface area of the affected layer.

3.3.2.9 Pink Ring There is no existing evidence that pink ring affects functionality. The presence of pink ring may be considered an indicator of process or design variation but is not a cause for rejection. The focus of concern should be the quality of the lamination bond.

3.3.2.10 Coverfilm Separations The coverfilm **shall** be uniform and free of coverfilm separations, such as wrinkles, creases, and soda strawing. Nonlamination **shall** be acceptable, provided such imperfections do not violate 3.3.2.4 and all of the following:

a. At random locations away from conductors, if each separation is no larger than 0.80 mm x 0.80 mm [0.0315 in x 0.0315 in] and is not within 1.0 mm [0.0394 in] of the board edge or the coverfilm opening. The total number of separations **shall not** exceed three in any 25 mm x 25 mm [0.984 in x 0.984 in] of coverfilm surface area.

b. The total separation **shall not** exceed 25% of the spacing between adjacent conductors.

c. There **shall** be no coverfilm nonlamination along the outer edges of the coverfilm.

3.3.2.11 Covercoat Requirements

3.3.2.11.1 Covercoat Coverage Covercoat coverage manufacturing variations resulting in skips, voids, and misregistration are subject to the following restrictions:

a. Metal conductors **shall not** be exposed or bridged by blisters in areas where covercoat is required. Touch up, if required to cover these areas with covercoat, **shall** be of a material that is compatible and of equal resistance to soldering and cleaning as the originally applied covercoat.

b. In areas containing parallel conductors, covercoat variations **shall not** expose adjacent conductors unless the area between the conductors is purposely left blank as for a test point or for some surface mount devices.

c. Covercoat need not be flush with the surface of the land. Misregistration of a covercoat-defined feature **shall not** expose adjacent isolated lands or conductors (see Figure 3-2).

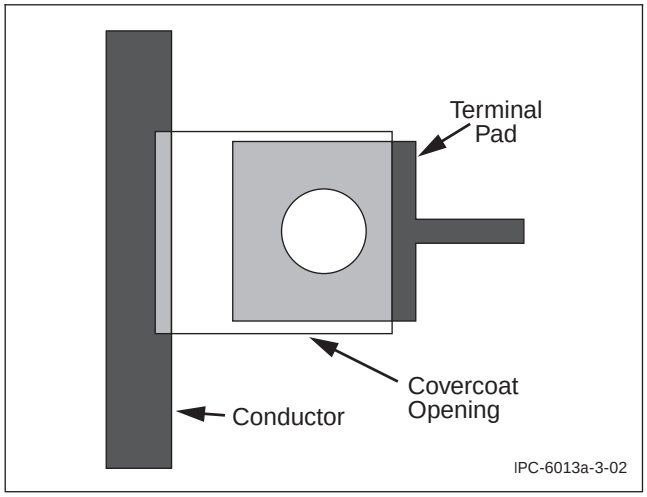

Figure 3-2 Unacceptable Covercoat Coverage

d. Covercoat is allowed on lands for plated-through holes to which solder connections are to be made, provided the external annular ring requirements for that class of products are not violated. Resist **shall not** encroach upon the barrel of this type of plated-through hole. Other surfaces, such as edge flexible printed wiring connector fingers and surface mount lands, **shall** be free of covercoat, except as specified. Covercoat is allowed in plated-through holes and vias into which no component lead is soldered, unless the procurement documentation requires that the holes be completely solder filled. Covercoat may tent or plug via holes as specified by the procurement documentation. Test points that are intended for assembly testing must be free of covercoat unless coverage is specified.

e. When a land contains no plated-through holes, as in the case of surface mount or ball grid array (BGA) lands, misregistration **shall not** cause encroachment of the covercoat on the land or lack of solder-resist-definition in excess of the following:

   a) On surface mount lands, misregistration **shall not** cause encroachment of the covercoat over the land area greater than 50 µm [1,969 µin] for a pitch ≥1.25 mm [0.04921 in]. Encroachment **shall not** exceed 25 µm [984 µin] for a pitch <1.25 mm [0.04921 in], and encroachment may occur on adjacent sides, but not on opposite sides of a surface mount land.

   b) On BGA lands, if the land is solder-resist-defined, misregistration may allow a 90° breakout of the covercoat on the land. If clearance is specified, no encroachment of the covercoat on the land is allowed, except at the conductor attachment.

   c) On BGA lands connected to via holes, which have coverlayer dams required, the dam **shall** be continuous without missing peeling or cracked coverlayer, allowing a bare metal path between the BGA land and the via.

f. Blistering **shall** be allowed to the following extent:

   a) Class 1: Does not bridge between conductors.

   b) Class 2 and Class 3: Two per side, maximum size 0.25 mm [0.00984 in] in longest dimension, does not reduce electrical spacing between conductors by more than 25%.

g. Pits and voids are allowed in nonconductor areas, provided they have adherent edges and do not exhibit lifting or blistering in excess of allowance in 3.3.2.11.1(f).

h. Coverage between closely spaced surface mount lands **shall** be as required by procurement documentation.

i. When design requires coverage to the flexible printed wiring edge, chipping or lifting of covercoat along the flexible printed wiring edge after fabrication **shall not** penetrate more than 1.25 mm [0.04291 in] or 50% of the distance to the closest conductor, whichever is less.

3.3.2.11.2 Covercoat Cure and Adhesion The cured covercoat **shall not** exhibit tackiness or blistering in excess of that permitted in 3.3.2.11.1(f). When tested in accordance with IPC-TM-650, Method 2.4.28.1, the maximum percentage of cured covercoat lifting from Coupon G identified in IPC-2221 **shall** be in accordance with Table 3-1.

Table 3-1 Covercoat Adhesion

Surface	Maximum Percentage Loss Allowed		
	Class 1	Class 2	Class 3
Bare Copper	10	5	0
Gold or Nickel	25	10	5
Base Laminate	10	5	0
Melting Metals (Tin-lead plating, fused tin-lead, and bright acid-tin)	50	25	10

3.3.2.11.3 Covercoat Thickness Covercoat thickness is not measured, unless specified on the procurement documentation. If a thickness measurement is required, instrumental methods may be used or an assessment may be

made using a microsection of the parallel conductors on Coupon E identified in IPC-2221.

3.3.2.12 Solder Wicking/Plating Penetration Solder wicking or other plating penetration **shall not** extend into a bend or flex transition area and **shall** meet the conductor spacing requirements. Solder wicking or other plating penetration **shall not** exceed the limits specified in Table 3-2.

Table 3-2 Solder Wicking/Plating Penetration Limits

Class 1	Class 2	Class 3
As agreed upon between user and supplier	0.5 mm [0.020 in] maximum	0.3 mm [0.012 in] maximum

See Figure 3-3, which displays penetration limits, defined as m1 and m2.

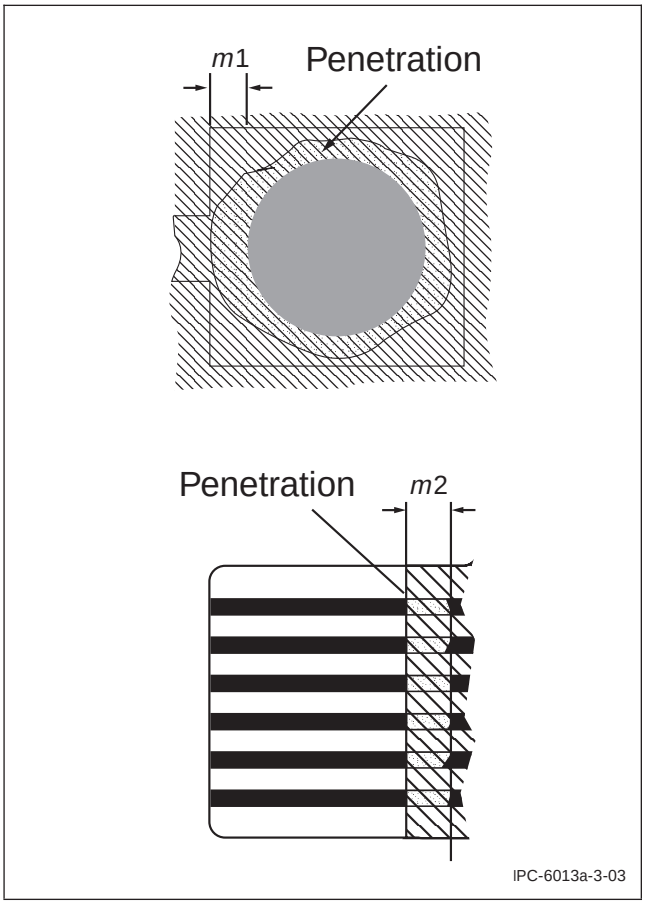

Figure 3-3 Solder Wicking and Plating Penetration

3.3.2.13 Stiffener A stiffener will be evaluated only as a mechanical support. Void-free bonding of the stiffener to the flexible printed wiring is not required. Specific requirements **shall** be as agreed upon between user and supplier.

3.3.3 Plating and Coating Voids in the Hole Plating and coating voids **shall not** exceed that allowed by Table 3-3.

3.3.4 Marking If required, each individual flexible printed board, qualification flexible printed board, and set of quality conformance test circuit strips (as opposed to each individual coupon) **shall** be marked. This marking is required in order to ensure traceability between the flexible printed wiring/test strips and the manufacturing history and to identify the supplier (i.e., logo). If size or space does not permit marking individual flexible printed wiring, bagging or tagging is permitted.

Table 3-3 Plating and Coating Voids Visual Examination

Material	Class 1	Class 2	Class 3
Copper	Three voids allowed per hole in not more than 10% of the holes	One void allowed per hole in not more than 5% of the holes	None
Finish Coating	Five voids allowed per hole in not more than 15% of the holes	Three voids allowed per hole in not more than 5% of the holes	One void allowed per hole in not more than 5% of the holes

Note 1: For Class 2 flexible printed wiring product, copper voids **shall not** exceed 5% of the hole length. For Class 1 flexible printed wiring product, copper voids **shall not** exceed 10% of the hole length. Circumferential voids **shall not** extend beyond 90° of the circumference.

Note 2: For Class 2 and 3 product, finished coating voids **shall not** exceed 5% of the hole length. For Class 1, finished coating voids **shall not** exceed 10% of the hole length. Circumferential voids **shall not** extend beyond 90° for Class 1, 2 or 3.

The marking **shall** be produced by the same process as used in producing the conductive pattern or by use of a permanent fungistatic ink or paint (see 3.2.10), LASER marker, or a vibrating pencil marking on a permanently attached label or metallic area provided for marking purposes.

Conductive markings, either etched copper or conductive ink (see 3.2.10), **shall** be considered as electrical elements of the circuit and **shall not** reduce the electrical spacing requirements. All markings **shall** be compatible with materials and parts, legible for all tests, and in no case affect flexible printed wiring performance.

Marking **shall not** cover areas of lands that are to be soldered (see IPC-A-600 for legibility requirements). In addition to this marking, the use of bar code marking is permissible. When used, date code **shall** be formatted per the supplier's discretion in order to establish traceability as to when the manufacturing operations were performed.

3.3.5 Solderability Only those flexible printed wiring that require soldering in a subsequent assembly operation require solderability testing. Solderability testing is not necessary for flexible printed wiring that does not require soldering. This **shall** be specified on the master drawing, as in the case where press-fit components are used. Flexible printed wiring to be used only for surface mount does not require hole solderability testing.

When required by the procurement documentation, accelerated aging for coating durability **shall** be in accordance

with J-STD-003. The category of durability **shall** be specified on the master drawing; however, if not specified, Category 2 **shall** be used. Specimens to be tested **shall** be conditioned, if required, and evaluated for surface and hole solderability using J-STD-003.

When solderability testing is required, consideration should be given to flexible printed wiring thickness and copper thickness. As both increase, the amount of time to properly wet the sides of the holes and the tops of the lands increases proportionately.

Note: Accelerated aging (steam aging) is intended for use on coatings of tin/lead, tin/lead solder, or tin, but not other final finishes.

3.3.6 Plating Adhesion The adhesion of the plating **shall** be tested in accordance with IPC-TM-650, Method 2.4.1.

There **shall** be no evidence of any portion of the protective plating or the conductor pattern foil being removed, as shown by particles of the plating or pattern foil adhering to the tape. If overhanging metal (slivers) breaks off and adheres to the tape, it is evidence of overhang or slivers, but not of plating adhesion failure.

3.3.7 Edge Board Contact, Junction of Gold Plate to Solder Finish Exposed copper/plating overlap between the solder finish and gold plate **shall** meet the requirements of Table 3-4. The exposed copper/plating or gold overlap may exhibit a discolored or gray-black area, which is acceptable (see 3.5.3.3).

Table 3-4 Edge Board Contact Gap

	Max. Exposed Copper Gap	Max. Gold Overlap
Class 1	2.5 mm [0.0984 in]	2.54 mm [0.0984 in]
Class 2	1.25 mm [0.04921 in]	1.25 mm [0.04291 in]
Class 3	0.8 mm [0.031 in]	0.8 mm [0.031 in]

3.3.8 Lifted Lands When visually examined in accordance with 3.3, there **shall** be no lifted lands on the deliverable (nonstressed) flexible printed wiring.

3.3.9 Workmanship Flexible printed wiring **shall** be processed in such a manner as to be uniform in quality and show no visual evidence of dirt, foreign matter, oil, fingerprints, tin/lead, or solder smear transfer to the dielectric surface, flux residue, and other contaminants that affect life, ability to assemble, and serviceability. Visually dark appearances in nonplated-through holes, which are seen when a metallic or nonmetallic semiconductive coating is used, are not foreign material and do not affect life or function. Flexible printed wiring **shall** be free of defects in excess of those allowed in this specification. There **shall** be no evidence of any lifting or separation of platings from the surface of the conductive pattern, or of the conductor from the base laminate in excess of that allowed. There **shall** be no loose plating slivers on the surface of the flexible printed wiring.

3.4 Dimensional Requirements The flexible printed wiring **shall** meet the dimensional requirements specified on the procurement documentation. All dimensional characteristics, such as flexible printed wiring periphery, thickness, cutouts, slots, notches, and edge contacts to connector key area, **shall** be as specified on the procurement documentation.

Automated inspection technology is allowed.

3.4.1 Hole Size and Hole Pattern Accuracy The hole size tolerance and hole pattern accuracy **shall** be as specified on the procurement documentation. Nodules or rough plating in plated-through holes **shall not** reduce the hole diameter below the minimum limits defined in the procurement documentation.

3.4.2 Etched Annular Ring and Breakout (Internal) The minimum internal annular ring **shall** meet the requirements of Table 3-5. Measurements for internal annular ring is from the inside of the drilled hole to the edge of the internal land as shown in Figure 3-4. Negative etchback is evaluated per 3.7.7. External pads of sequentially laminated structures are considered as an external layer and are evaluated in process prior to additional lamination(s) (see 3.4.3). Microsection analysis is performed per 3.7.2 (see Figures 3-6 and 3-7).

Internal registration may be assessed by nondestructive techniques other than microsection, such as, special patterns, probes, and/or software which are configured to provide information on the interpolated annular ring remaining and pattern skew.

Techniques include, but are not limited to the following:

- The optional F coupon.
- Custom designed electrically testable coupons.
- Radiographic (x-ray) techniques.
- Horizontal microsection.
- CAD/CAM data analysis as correlated to pattern skew by layer.

Note: It is recommended that microsectioning or statistical sampling is used to verify correlation of the approved technique, and a calibration standard is established for the specific technique employed.

3.4.3 Etched Annular Ring (External) The minimum external annular ring **shall** meet the requirements of Table 3-5. The measurement of the annular ring on external layers is from the inside surface (within the hole) of the plated

Table 3-5 Minimum Etch Annular Ring

Characteristic	Class 1	Class 2	Class 3
EXTERNAL Plated-through holes	Not greater than 180° breakout of hole from land when visually assessed.[1] The land/conductor junction **shall not** be reduced below the allowable width reduction in 3.5.1.1.	Not greater than 90° breakout of hole from land when visually assessed and a 50 µm [0.0020 in] annular ring for at least 270° of the circumference.[1] The land/conductor junction **shall not** be reduced below the allowable width reduction in 3.5.1.1. The conductor junction should never be <50 µm [0.0020 in] or the minimum line width, whichever is smaller.	The minimum annular ring **shall** be 50 µm [0.0020 in]. The land/conductor junction **shall not** be reduced below the allowable width reduction in 3.5.1.1. The minimum external annular ring may have 20% reduction of the minimum annular ring in isolated areas due to defects such as pits, dents, nicks, pinholes, or splay in the annular ring of isolated areas.
INTERNAL Plated-through holes	Hole breakout is allowed provided the land/conductor junction is not reduced below the allowable width reduction in 3.5.1.1.[1]	Hole breakout is allowed provided the land/conductor junction is not reduced below the allowable width reduction in 3.5.1.1.[1]	The minimum functional internal annular ring **shall** be 25 µm [0.00098 in].
EXTERNAL Unsupported holes	Not greater than 90° breakout of hole from land when visually assessed.[1] The land/conductor junction **shall not** be reduced below the allowable width reduction in 3.5.3.1.	Not greater than 90° breakout of hole from land when visually assessed.[1] The land/conductor junction **shall not** be reduced below the allowable width reduction in 3.5.3.1.	The minimum annular ring **shall** be 150 µm [0.00591 in]. The minimum external annular ring may have a 20% reduction of the minimum annular ring in isolated areas due to defects such as pits, dents, nicks, pinholes or splay in the annular ring of isolated areas.

[1] Minimum lateral spacing **shall** be maintained.
Note: (See Figure 3-6 and 3-7 for land breakout and conductor width reduction at land.)

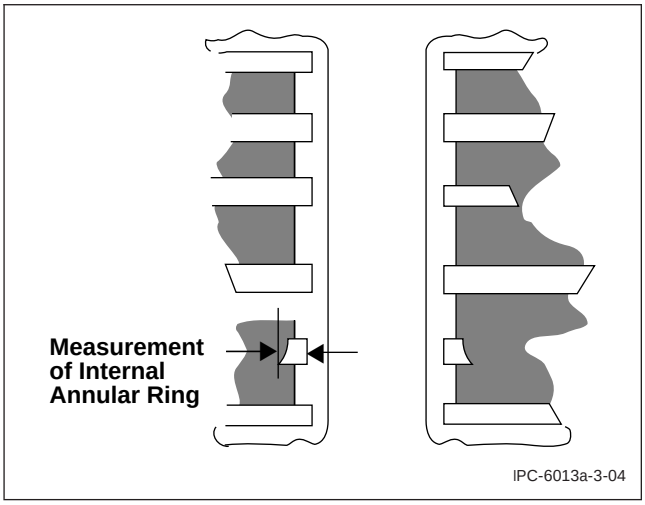

Figure 3-4 Annular Ring Measurement (Internal)

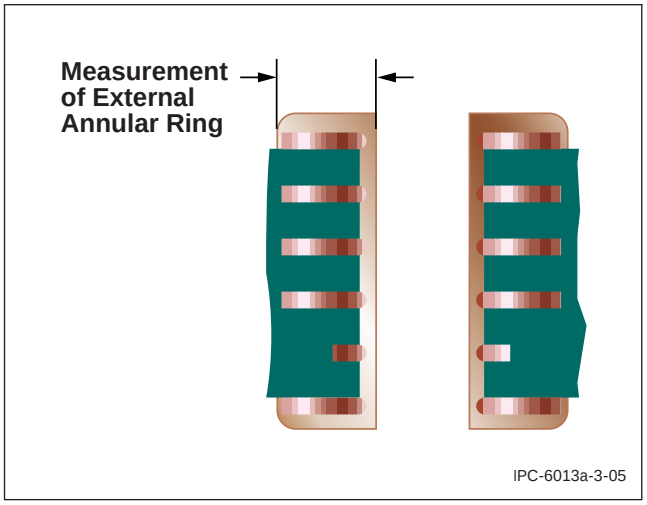

Figure 3-5 Annular Ring Measurement (External)

hole, or unsupported hole, to the outer edge of the annular ring on the surface of the board as shown in Figure 3-5. For Class 1 and 2, external plated through holes identified as vias (not having a component) can have up to 90° breakout of the annular ring. The breakout **shall not** occur at the conductor/land intersection and the hole **shall** meet the requirements of 3.7.8 and 3.7.9. The finished board with the related breakout **shall** meet the electrical requirements of 3.9.2 (see Figures 3-6 and 3-7).

3.4.3.1 Solderable Annular Ring (External) Adhesive squeeze-out, solder mask misregistration, and/or coverlayer on land areas are permitted; however, the minimum solderable annular ring **shall** meet the requirements of Table 3-7.

When examined in accordance with 3.3, the measurement of the annular ring on external layers is from the inside surface (within the hole) of the plated or unsupported hole to the outer edge of the annular ring on the surface of the flexible printed wiring. Plated-through holes identified as vias can have up to 90° breakout of the annular ring if it does not occur at the conductor and land intersection.

3.4.3.2 Squeeze-Out of Adhesive of Coverlayer and Ooze-Out of Covercoat Squeeze-out (j) of coverlayer adhesive or ooze-out of covercoat on the foil surface, as

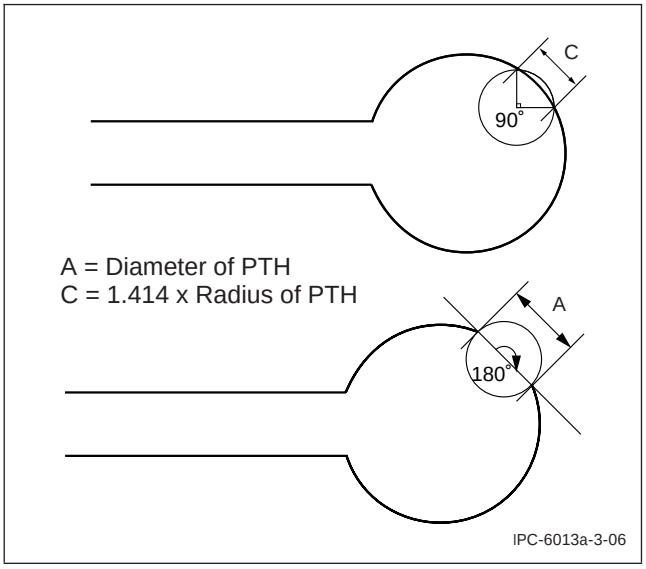

Figure 3-6 Breakout of 90° and 180°

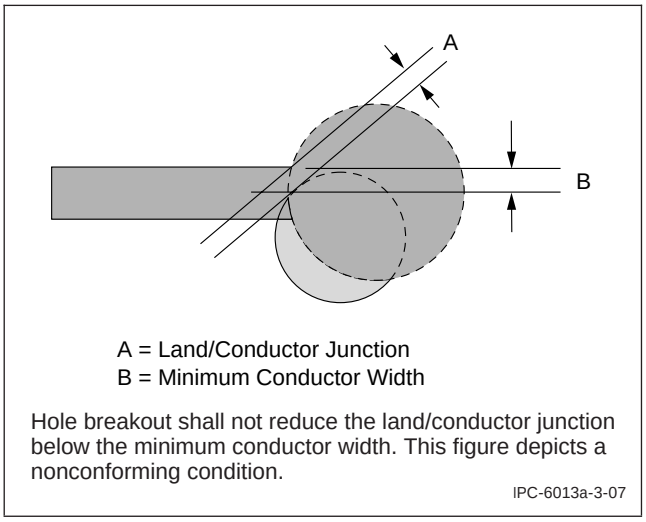

Figure 3-7 Conductor Width Reduction

shown in Figure 3-8, **shall** meet the requirements of Table 3-6. On the land area, as shown in Figure 3-8, the minimum solderable annular ring (k) **shall** meet the requirements of Table 3-7.

3.4.3.3 Stiffener Access Hole Registration of the stiffener to the flexible printed wiring **shall not** reduce external annular ring requirements below that specified in 3.4.3.

3.4.4 Bow and Twist (Individual Rigid or Stiffener Portions Only) Unless otherwise specified in the procurement documentation, when designed in accordance with IPC-2221 and IPC-2223, the rigid or stiffener portions of the flexible printed wiring **shall** have a maximum bow and twist of 0.75% for applications that use surface mount components and 1.5% for all other applications. For any product grouped in panels for assembly purposes, bow and twist requirements will need to be determined by the user and supplier.

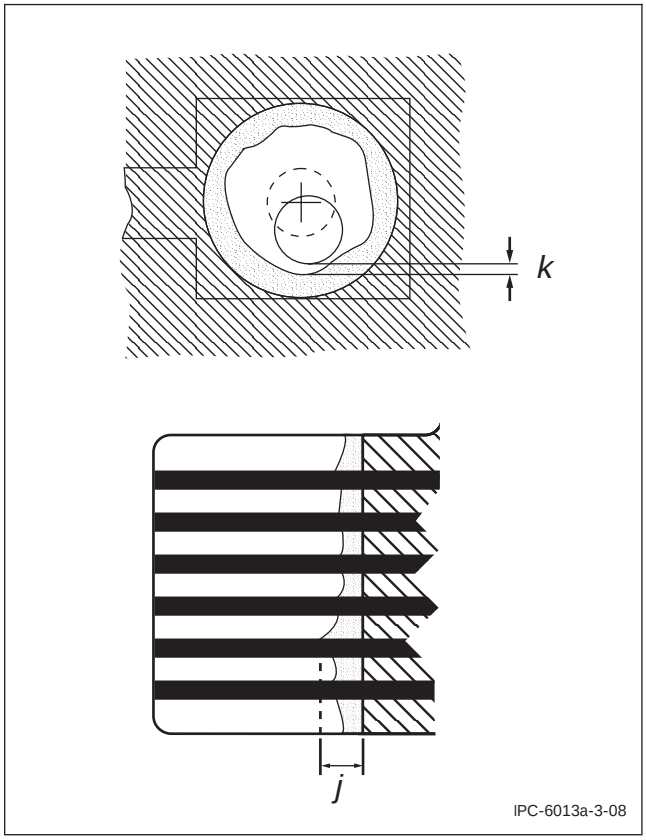

Figure 3-8 Squeeze-Out of Cover Film Adhesive and Ooze-Out of Covercoat

Table 3-6 Allowable Squeeze-Out of Coverlayer Adhesive and Ooze-Out of Covercoat

Class	70 µm Foil and Below	Above 70 µm Foil
1 and 2	≤0.3 mm [0.0118 in]	≤0.5 mm [0.0197 in] or as agreed upon with the manufacturer
3	≤0.2 mm [0.0079 in]	≤0.4 mm [0.0157 in] or as agreed upon with the manufacturer

Table 3-7 Minimum Solderable Annular Ring on Land Area

Class	Solderable Annular Ring
1	A solderable annular ring for at least 240° of the circumference.
2	A 0.05 mm [0.00197 in] solderable annular ring for at least 270° of the circumference.
3	A 0.05 mm [0.00197 in] solderable annular ring for 360° of the circumference.

Bow, twist, or any combination thereof **shall** be determined by physical measurement and percentage calculation in accordance with IPC-TM-650, Method 2.4.22, which describes four procedures used to determine bow and twist of either cut to size panels or finished flex or rigid-flex printed boards including single-sided, double-sided and multilayer.

3.5 Conductor Definition All conductive areas on flexible printed wiring, including conductors, lands, and

planes, **shall** meet the visual and dimensional requirements of 3.5.1 through 3.5.3.7. The conductor pattern **shall** be as specified in the procurement documentation. When not specified on the master drawing, the minimum conductor width **shall** be 80% of the conductor pattern supplied in the procurement documentation. When not specified on the master drawing, the minimum conductor thickness **shall** be in accordance with 3.7.12 and 3.7.13. Verification of dimensional attributes **shall** be performed in accordance with IPC-A-600. AOI inspection methods are allowed. Internal conductors are examined during internal layer processing prior to multilayer lamination.

3.5.1 Conductor Imperfections The conductive pattern **shall** contain no cracks, splits, or tears. The physical geometry of a conductor is defined by its width x thickness x length. Any combination of defects specified in 3.5.1.1 and 3.5.1.2 **shall not** reduce the equivalent cross-sectional area (width x thickness) of the conductor by more than 20% of the minimum value (minimum thickness x minimum width) for Class 2 and Class 3 and 30% of the minimum value for Class 1. The total combination of defect area lengths on a conductor **shall not** be >10% of the conductor length or 25 mm [0.984 in] for Class 1 or 13 mm [0.512 in] for Class 2 or Class 3, whichever is less.

3.5.1.1 Conductor Width Reduction Allowable reduction of the minimum conductor width (specified or derived) due to isolated defects (i.e., edge roughness, nicks, pinholes, and scratches), which expose base material, **shall not** exceed 20% of the minimum conductor width for Class 2 and Class 3 and 30% of the minimum conductor width for Class 1.

3.5.1.2 Conductor Thickness Reduction Allowable reduction of the minimum conductor thickness due to isolated defects (i.e., edge roughness, nicks, pinholes, depressions, and scratches) **shall not** exceed 20% of the minimum conductor thickness for Class 2 and Class 3 and 30% of the minimum conductor thickness for Class 1.

3.5.2 Conductor Spacing The conductor spacing **shall** be within the tolerance specified on the master drawing. Minimum spacing between the conductor and the edge of the flexible printed wiring **shall** be as specified on the master drawing. Minimum conductor spacing may be reduced in isolated areas per Table 3-8.

Table 3-8 Conductor Spacing Requirements

Class 1 & Class 2	Class 3
Minimum conductor spacing may be reduced an additional 30% due to conductor edge roughness, spikes, etc.	Minimum conductor spacing may be reduced an additional 20% due to conductor edge roughness, spikes, etc.

If minimum spacing is not specified, the allowed reduction in the nominal conductor spacings shown in the engineering documentation due to processing **shall** be 20% for Class 3 and 30% for Class 1 and Class 2 (minimum product spacing requirements as previously stated apply).

3.5.3 Conductive Surfaces

3.5.3.1 Nicks and Pinholes in Ground or Voltage Planes For nicks and pinholes in ground or voltage planes, the maximum size allowed **shall** be 1.0 mm [0.0394 in] for Class 2 and Class 3, with no more than four per side per 625 cm^2 [96.88 in^2]. For Class 1, the maximum size may be 1.5 mm [0.0591 in] with no more than six per side per 625 cm^2 [96.88 in^2].

3.5.3.2 Surface Mount Lands Defects such as nicks, dents, and pinholes along the edge of the land **shall not** exceed 20% of either the length or width of the land for Class 2 or Class 3 flexible printed wiring or 30% for Class 1. Defects internal to the land **shall not** exceed 10% of the length or width of the land for Class 2 or Class 3 flexible printed wiring or 20% for Class 1.

3.5.3.3 Edge Connector Lands On gold or other noble metal-plated edge flexible printed wiring connector lands, except as noted below, the insertion or contact area **shall** be free of the following:

- Cuts or scratches that expose nickel or copper.
- Solder splashes or tin-lead plating.
- Nodules or metal bumps that protrude above the surface.

Pits, dents, or depressions are acceptable if they do not exceed 0.15 mm [0.00591 in] in their longest dimension and there are not more than three per land and do not appear on more than 30% of the lands. The imperfection limits do not apply to a band 0.15 mm [0.00591 in] wide around the perimeter of the land, including the insertion area.

3.5.3.4 Dewetting Dewetting on conductors, areas of solder connection, and ground or voltage planes is allowed to the extent listed below:

a) Allowed for conductors and planes not intended for solder connection for all classes.

b) Each individual area of solder connection: Class 1, 15%; Class 2 and Class 3, 5%.

3.5.3.5 Nonwetting For tin, tin/lead reflowed or solder coated surfaces, nonwetting is not permitted on any conductive surface where a solder connection is required.

3.5.3.6 Final Finish Coverage Final finish **shall** meet the solderability requirements of J-STD-003. Exposed copper on areas not to be soldered is permitted on 5% of the conductor surfaces for Class 1, 2 and 3. Coverage does not apply to vertical conductor edges.

3.5.3.7 Conductor Edge Outgrowth There **shall** be no evidence of outgrowth on edges of conductors that have been solder coated or tin-lead plated and fused when tested in accordance with IPC-TM-650, Method 2.4.1 (see IPC-2221).

3.6 Physical Requirements

3.6.1 Bending Test The bending test **shall** conform to Figure 3-9, unless otherwise agreed to by the user. The bending test requirements **shall** be as specified on the appropriate document/drawing. See IPC-2223 for guidance on minimum bend radii. The following parameters **shall** be specified as a minimum:

- Direction of bend (a).
- Degree of bend (b).
- Number of bend cycles (c).
- Diameter of mandrel (d).
- Points of application to be specified by user.

Bend cycle is defined as taking one end of the specimen and bending it around a mandrel and then bending back to the original starting position, traveling 180° in one direction and 180° in the opposite direction. A bend cycle may also be defined as bending (using opposite ends) the ends toward each other (bend the same direction) and then bending them back to the original starting position, with each end traveling 90° in one direction and 90° in the opposite direction.

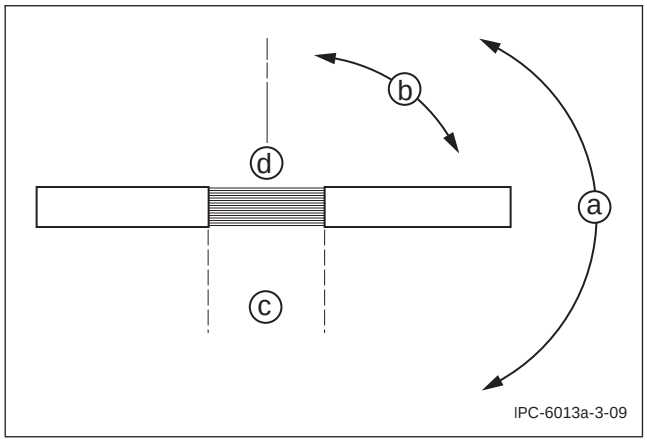

Figure 3-9 Bending Test

The specified number of bend cycles **shall** be performed with the mandrel placed in contact with the specimen on one side and then again with the mandrel placed in contact with the specimen on the opposite side. After completion of the bending test in both directions, the flexible or rigid-flexible printed wiring **shall** be tested for electrical defects in accordance with 3.9 and **shall** meet the requirements of 3.3.

3.6.2 Flexible Endurance Flexible endurance testing **shall** be carried out using IPC-TM-650, Method 2.4.3.1; as an alternate, IPC-TM-650, Method 2.4.3 may be used. Flexible endurance testing can also be accomplished with special test equipment specific to the circuit application.

The flexibility endurance test requirements **shall** be specified in the appropriate document/drawing. The following parameters **shall** be specified as a minimum:

- Number of flex cycles.
- Diameter of the bend mandrels or separation of the loop-defining plates.
- Flexing rate.
- Points of application.
- Travel of loop.

The method for determining end of life is an electrical discontinuity in a monitored daisy-chain.

3.6.3 Bond Strength (Unsupported Lands) When flexible printed wiring is tested in accordance with IPC-TM-650, Method 2.4.20, the unsupported land **shall** withstand 1.86 kg pull or 35 kg/cm^2 [498 PSI], whichever is less, after subjection to five cycles of soldering and unsoldering. Calculations of land area of the unsupported hole do not include the area occupied by the hole.

3.6.4 Bond Strength (Stiffener) Using a sharp instrument (i.e., scalpel or razor blade), cut a pattern approximately 13 mm [0.512 in] wide by 76 mm [2.99 in] long through the flexible printed wiring to the stiffener so that approximately half way through the peeling operation the sample will be perpendicular to the pull.

Pull at a rate of 57 mm/minute [2.24 in/minute]. Take readings at the beginning, middle, and end of the pull and average these readings to determine acceptability. The peel strength between the flexible printed wiring and the stiffener **shall** be a minimum of 1.4 kg per 25 mm [0.984 in] width.

3.7 Structural Integrity Flexible printed wiring **shall** meet structural integrity requirements for thermally stressed (after solder float) evaluation coupons specified in 3.7.2. Although the A and B or A/B coupons are assigned for this test, production boards may be used in lieu of the A and B or A/B coupons and are preferred for product that contains surface mount and vias or surface mount mixed with through-hole technology. Holes selected **shall** be equivalent to those specified for quality conformance test coupons.

The production flexible printed wiring and all other coupons in the quality conformance test circuitry that contain plated-through holes **shall** be capable of meeting the requirements of this section. Structural integrity **shall** be used to evaluate test specimens from Type 2 through Type 4 flexible printed wiring by microsectioning techniques.

Characteristics not applicable to Type 2 flexible printed wiring are not evaluated. Dimensional measurements that are only possible through the use of microsectioning techniques are also defined in this section. Blind and buried vias **shall** meet the requirements of plated-through holes.

The evaluation of all properties and requirements **shall** be performed on the thermally stressed coupon and all requirements must be met; however, per supplier election, certain properties and conditions as defined below may be evaluated in a coupon(s) that has not been thermally stressed.

- Copper voids
- Plating folds/inclusions
- Burrs and nodules
- Glass fiber protrusion
- Wicking
- Final coating plating voids
- Etchback
- Negative etchback
- Plating/coating thickness
- Internal and surface copper layer or foil thickness
- Laminate (rigid)

3.7.1 Thermal Stress Testing The specimens should be conditioned by baking at 120 °C to 150 °C [248 °F to 302 °F] for a recommended minimum of six hours to remove moisture. Thicker or more complex specimens may require longer baking times. After conditioning, place the specimens in a desiccator on a ceramic plate to cool to room temperature. Specimens **shall** be thermally stressed in accordance with IPC-TM-650, Method 2.6.8, test condition A (289 °C [552 °F]) for polyimide, and test condition C (235 °C [455 °F]) for polyester.

Following stress, specimens **shall** be microsectioned. Microsectioning **shall** be accomplished per IPC-TM-650, Method 2.1.1 or 2.1.1.2, on test specimens, coupons, or production flexible printed wiring. A minimum of three holes or vias **shall** be inspected in the vertical cross section. The grinding and polishing accuracy of the microsection **shall** be such that the viewing area of each of the three holes is within 10% of the drilled diameter of the hole.

Plated-through holes **shall** be examined for foil and plating integrity at a magnification of 100X ± 5%. Referee examinations **shall** be accomplished at a magnification of 200X ± 5%. Each side of the hole **shall** be examined independently. Examination for laminate thickness, foil thickness, plating thickness, lay-up orientation, lamination and plating voids, etc., **shall** be accomplished at magnifications specified above. Plating thickness below 1 µm [39.4 µin] **shall not** be measured using metallographic techniques.

3.7.2 Requirements for Microsectioned Coupons When examined in microsection, the coupons **shall** meet the requirements of Table 3-9 and 3.7.3 through 3.7.16.

3.7.3 Flexible Laminate Integrity For Class 1, Class 2, and Class 3 flexible printed wiring, there **shall** be no adhesive voids in Zone B (see Figure 3-12) in excess of 0.50 mm [0.0197 in]. Multiple voids between two adjacent plated-through holes in the same plane **shall not** have a combined length exceeding the above limit.

3.7.4 Rigid Laminate Integrity Laminate voids/cracks in Zone A are acceptable (see Figure 3-12). Voids/cracks that originate in Zone A and extend into Zone B or are entirely in Zone B **shall not** be in excess of 0.08 mm [0.00315 in] for Class 2 or Class 3 products and 0.15 mm [0.00591 in] for Class 1 products. Multiple voids/cracks between two adjacent plated-through holes in the same plane **shall not** have a combined length that exceeds these limits. Cracks between two uncommon conductors in either the horizontal or vertical direction **shall not** decrease the minimum dielectric spacing.

3.7.5 Etchback (Type 3 and Type 4 Only) When specified on the procurement documentation, flexible printed wiring **shall** be etched back for the lateral removal of resin and/or glass fibers from the drilled hole walls prior to plating. The etchback **shall** be between 0.003 [0.000118 in] mm (copper exposed) and 0.08 mm [0.00315 in] (maximum material removed). Shadowing is permitted on one side of each land (see Figure 3-13).

Note: Due to the various materials used in the construction of rigid-flex printed wiring, varying degrees of etchback amongst the various materials is to be expected in the finished product.

3.7.6 Smear Removal (Type 3 and Type 4 Only) Smear removal is the removal of resin debris that results from the formation of the hole. Smear removal **shall** be sufficient to completely remove resin from the surface of the conductor interface (see Figure 3-14).

3.7.7 Negative Etchback Negative etchback **shall not** exceed the dimensions in Figure 3-15 when measured as shown in Figure 3-15. Negative etchback **shall not** be allowed when etchback has been specified on the procurement documentation.

3.7.8 Plating Integrity Plating integrity in the plated-through holes **shall** meet the requirements detailed in Table 3-9. For Class 2 and Class 3 products, there **shall** be no separation of plating layers (except as noted in Table 3-9), no plating cracks, and internal interconnections **shall** exhibit no separation or contamination between plated-through hole wall and internal layers. Metal core or thermal

Table 3-9 Plated-Through Hole Integrity After Stress

Property	Class 1	Class 2	Class 3
Copper voids	Three voids allowed per hole. Voids in the same plane are not allowed. No void **shall** be longer than 5% of flexible printed wiring thickness. No circumferential voids are allowed.	One void allowed per test specimen, provided the additional microsection criteria of 3.7.9 are met.	One void allowed per test specimen, provided the additional microsection criteria of 3.7.9 are met.
Plating folds/inclusions[1]	Must be enclosed		
Burrs[1,2] and nodules[1]	Allowed if minimum hole diameter is met	Allowed if minimum hole diameter met	Allowed if minimum hole diameter met
Glass fiber protrusion[1,2]	Allowed if minimum hole diameter is met		
Wicking	100 µm [3,937 µin] maximum	80 µm [3,150 µin] maximum	50 µm [1,969 µin] maximum
Interplane inclusions (inclusions at the interface between internal lands and through-hole plating)	Allowed on only one side of hole wall at each land location on 20% of each available land	None allowed	
Internal foil cracks[3]	''C'' cracks allowed on only one side of hole, provided it does not extend through foil thickness	None allowed	
External foil cracks[3] (type ''A'' ''B'' and ''D'' cracks)	''D'' cracks not allowed ''A'' and ''B'' cracks allowed	''D'' and ''B'' cracks not allowed ''A'' cracks allowed	
Barrel/Corner cracks[3] (type ''E'' and ''F'' cracks)	None allowed		
Interplane separation (separation at the interface between internal lands and through-hole plating)	Allowed on only one side of hole wall at each land location on 20% of each available land	None allowed	
Separations along the vertical edge of the external land(s)	Allowed (see Figure 3-10), provided it does not extend beyond the vertical edge of the external copper foil		
Plating separation	Allowed at knee, maximum length 125 µm [4921 µin]	None allowed	
Hole wall dielectric/ plated barrel separation	Acceptable, provided dimensional and plating requirements are met		
Lifted lands after thermal stress or rework simulation	Allowed, provided the finished flexible printed wiring meets the visual criteria of 3.3		

[1] The minimum copper thickness in Table 1-1 must be met.
[2] As measured from the end of the protrusion into the hole.
[3] Copper crack definition: See Figure 3-11.
''A'' crack = A crack in the external foil.
''B'' crack = A crack that does not completely break plating (minimum plating remains).
''C'' crack = A crack in the internal foil.
''D'' crack = A crack in the external foil and plating - complete break in foil and plating.
''E'' crack = A barrel crack in plating only.
''F'' crack = A corner crack in the plating only.

planes, when used as electrically functional circuitry, **shall** meet the above requirements when made from copper, but those made from dissimilar metals may have small spots or pits at their junction with the hole wall plating. Those areas of contamination or inclusions **shall not** exceed 50% of each side of the interconnection or occur in the interface of the copper cladding on the core and the copper plating in the hole wall when viewed in the microsection evaluation.

3.7.9 Plating Voids Class 1 product **shall** meet the requirements for plating voids established in Table 3-9. For Class 2 and Class 3 products, there **shall** be no more than one void per test specimen, and the following criteria must be met:

- There **shall** be no more than one plating void per test specimen, regardless of length or size.
- There **shall** be no plating void in excess of 5% of the total flexible printed wiring thickness.
- There **shall** be no plating voids evident at the interface of an internal conductive layer and the plated-through hole wall.
- Circumferential plating voids are not allowed.

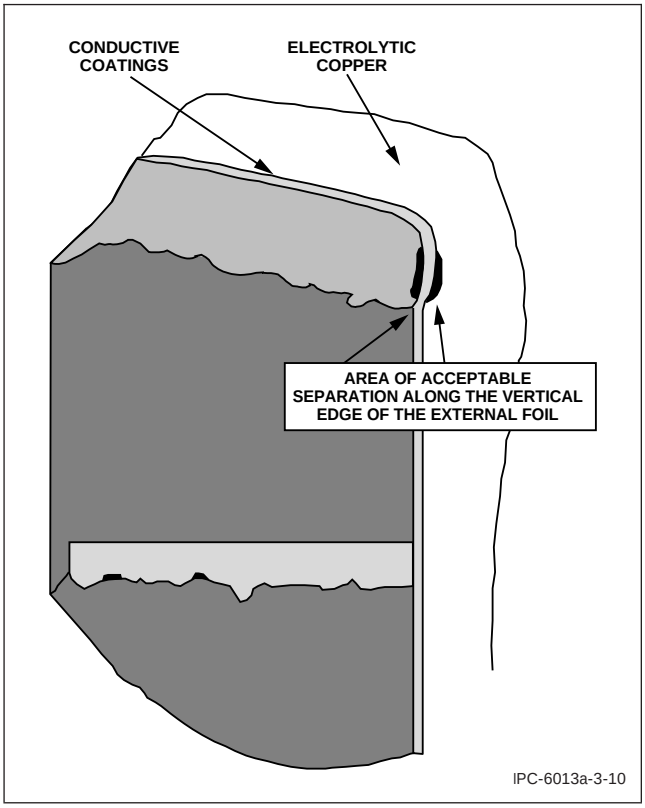

Figure 3-10 Separation at External Foil

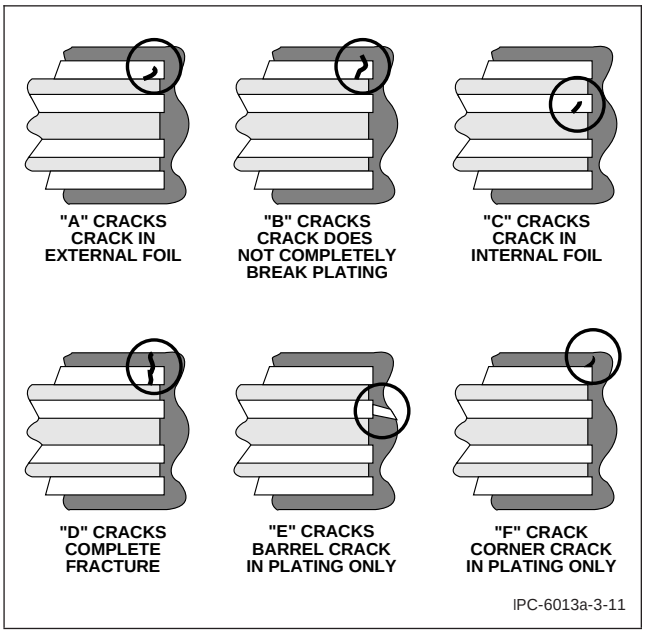

Figure 3-11 Crack Definition

If a void meeting this criteria is detected during evaluation of a microsection, a second test specimen **shall** be microsectioned from the same panel to determine if the defect is random. If the second test specimen has no plating voids, the product that the second test specimen represent is considered acceptable; however, if a plating void is present in the second microsectioned test specimen, the product **shall** be considered nonconforming.

3.7.10 Annular Ring (Internal) Internal annular ring, if not determined by the techniques in 3.4.2, **shall** be measured by microsection to verify conformance to Table 3-5 as shown in Figure 3-4.

3.7.11 Plating/Coating Thickness Based on microsection examination or the use of suitable electronic measuring equipment, plating/coating thickness **shall** meet the requirements of Table 1-1 or be as specified on the procurement documentation. Measurements in the plated-through hole **shall** be reported as an average thickness per side of the hole. Isolated thick or thin sections **shall not** be used for averaging. Isolated areas of reduced copper thickness **shall** be measured and evaluated to the copper plating void rejection criteria specified in 3.3.3.

3.7.12 Minimum Layer Copper Foil Thickness The minimum copper thickness after processing **shall** be in accordance with Table 3-10 for all classes. When the procurement documentation specifies a minimum copper thickness for conductors, the conductor **shall** meet or exceed that minimum thickness.

3.7.13 Minimum Surface Conductor Thickness The minimum total (copper foil plus copper plating) conductor thickness after processing **shall** be in accordance with Table 3-11. When the procurement documentation specifies a minimum copper thickness for external conductors, the specimen **shall** meet or exceed that minimum thickness.

3.7.14 Metal Cores All metal core printed boards, which have clearance between the plated-through holes and the metal core, **shall** require a horizontal microsection prepared to view the metal core/hole fill insulation. Specimens **shall** have been subjected to thermal stress in accordance with 3.7.1 prior to microsectioning. Wicking, radial cracks, lateral spacing, or voids in the hole-fill insulation material **shall not** reduce the electrical spacing between adjacent conductive surfaces to <0.100 mm [0.00394 in]. Wicking and/or radial cracks **shall not** exceed 0.75 mm [0.0295 in] from the plated-through hole edge into the hole-fill.

3.7.15 Dielectric Thickness The minimum dielectric spacing **shall** be specified on the procurement documentation.

3.7.16 Resin Fill of Blind and Buried Vias There is no fill requirement for blind and buried vias.

3.8 Rework Simulation When specified, printed boards or test coupons **shall** be tested in accordance with IPC-TM-650, Method 2.4.36, then microsectioned and examined in accordance with 3.7. Lifted lands are allowed. Rework simulation is not required for flexible printed boards that

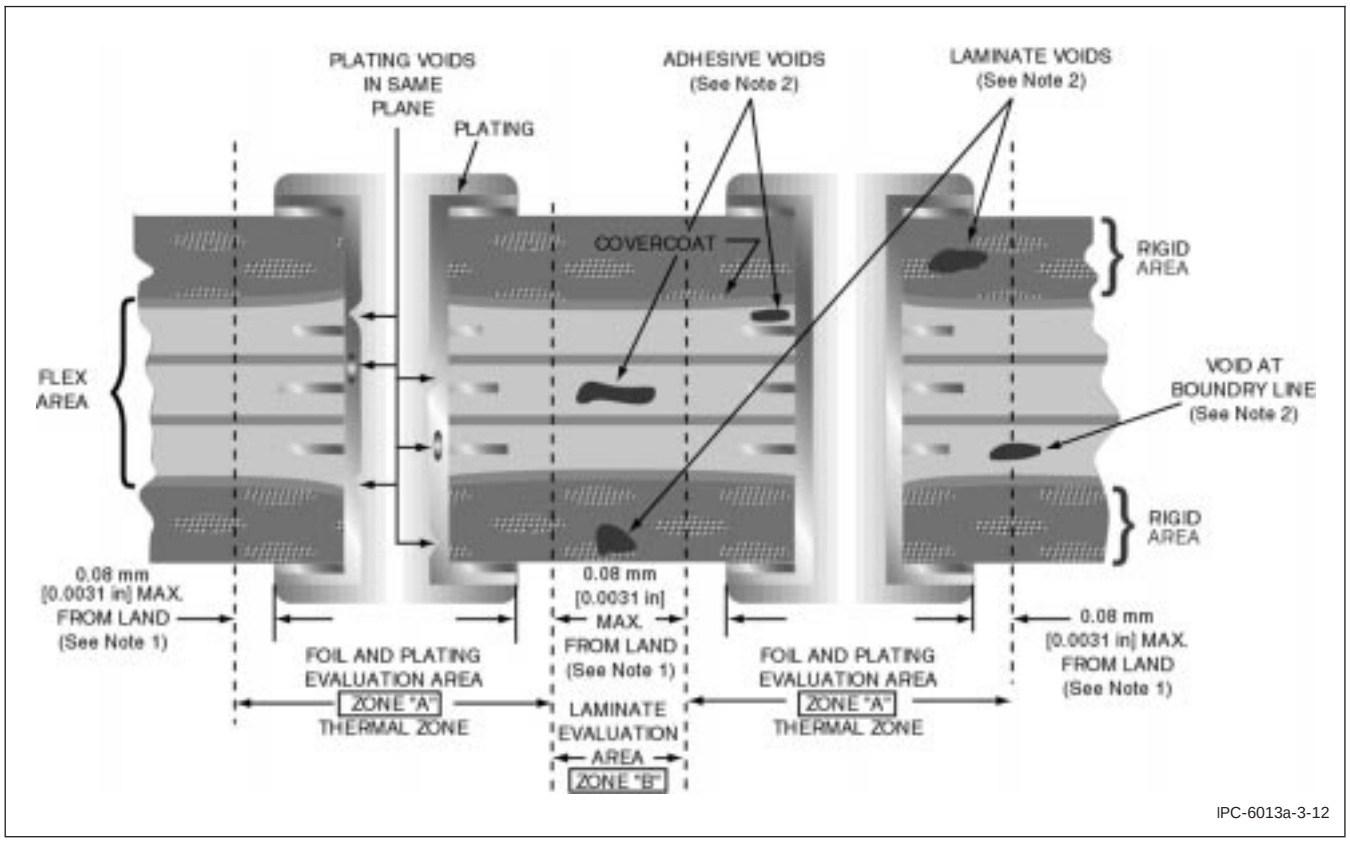

Figure 3-12 Typical Microsection Evaluation Specimen (Three Plated-Through Holes)

Notes:

1. The thermal zone extends 0.08 mm [0.0031 in] beyond the end of the land, either internal or external, extending furthest into the laminate area.
2. Laminate or adhesive anomalies or imperfections (such as laminate voids, adhesive voids, laminate cracks, delamination/blistering, etc.) **shall** be evaluated in both Zone A and Zone B prior to thermal stress or rework simulation. Zone A **shall not** be evaluated for these laminate or adhesive anomaly conditions after thermal stress or rework simulation.

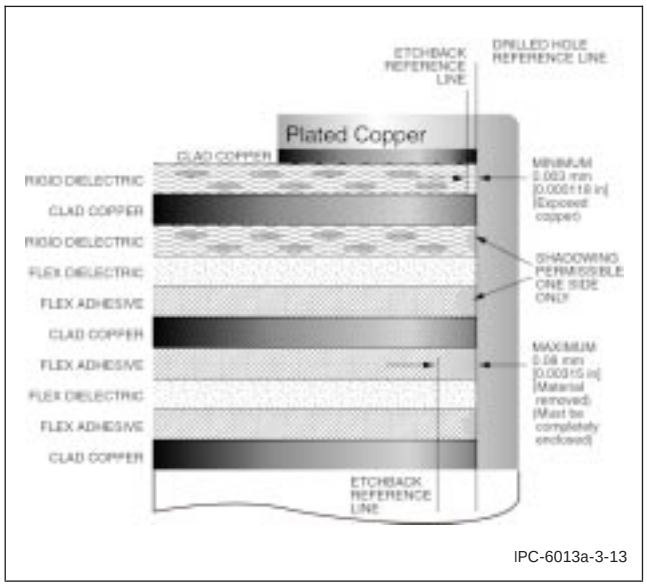

Figure 3-13 Etchback Depth Allowance

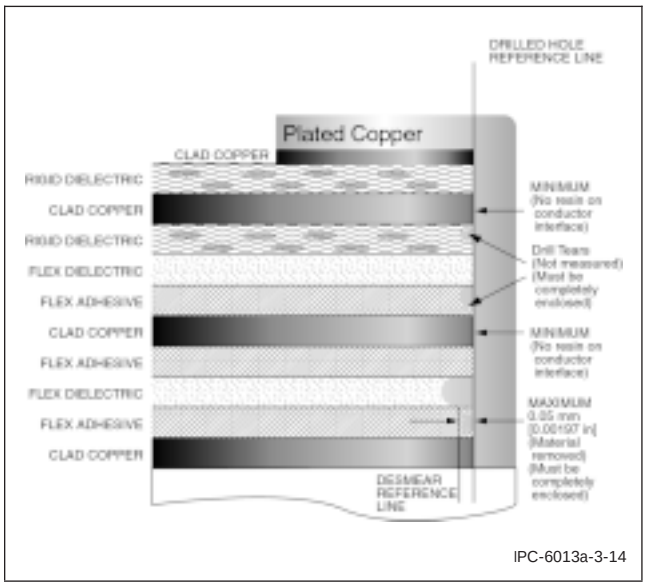

Figure 3-14 Smear Removal Allowance

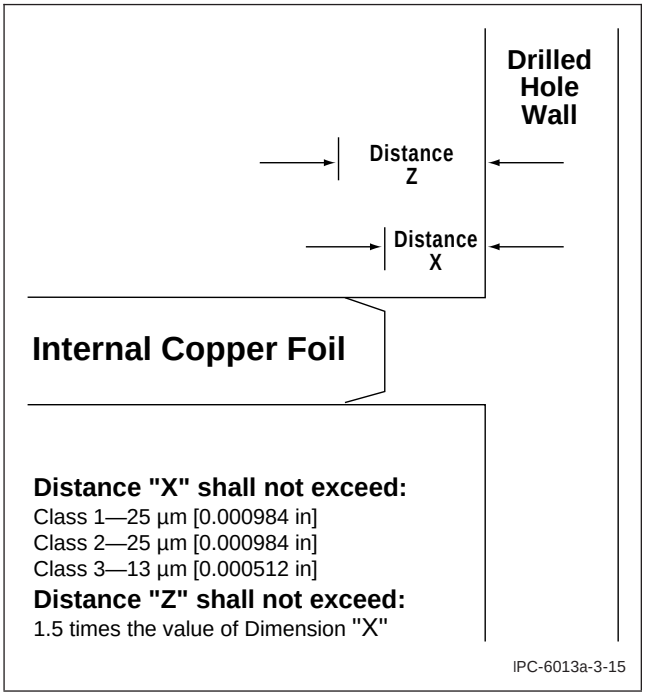

Figure 3-15 Negative Etchback

Table 3-10 Conductor Thickness After Processing

Designator	Weight	Nominal Starting Foil Thickness (µm) [µin]	Minimum Final Finish after Processing (µm) [µin]
E	1/8 oz.	5.0 [197]	3.1 [122]
Q	1/4 oz.	9.0 [354]	6.2 [244]
T	3/8 oz.	12.0 [472]	9.3 [366]
H	1/2 oz.	17.2 [677]	13.4 [528]
1	1 oz.	34.3 [1350]	27.9 [1098]
2	2 oz.	68.6 [2680]	58.7 [2311]
3	3 oz.	103.0 [4055]	89.6 [3528]
4	4 oz.	137.0 [5394]	119.5 [4705]
	Above 4 oz.		4 µm [157 µin] below minimum thickness listed for that foil thickness in IPC-4562

do not contain holes used for component mounting (i.e., surface mount or BGA only).

3.9 Electrical Requirements When tested as specified in Table 3-12, the flexible printed wiring **shall** meet the electrical requirements detailed in 3.9.1 through 3.9.4.

3.9.1 Dielectric Withstanding Voltage Applicable coupons tested as outlined below **shall** meet the requirements of Table 3-12, without flashover, sparkover, or breakdown between conductors or conductors and lands. The dielectric withstanding voltage test **shall** be performed in accordance

Table 3-11 External Conductor Thickness After Plating

Designator	Weight	Nominal Foil Thickness (µm) [µin]	Minimum Surface Conductor Thickness after Processing (µm) [µin]	
			Class 1 & 2	Class 3
E	1/8 oz.	5.0 [197]	23.1 [909]	28.1 [1106]
Q	1/4 oz.	9.0 [354]	26.2 [1031]	31.2 [1228]
T	3/8 oz.	12.0 [472]	29.3 [1154]	34.3 [1350]
H	1/2 oz.	17.2 [677]	33.4 [1315]	37.4 [1472]
1	1 oz.	34.3 [1350]	47.9 [1886]	53.9 [2122]
2	2 oz.	68.6 [2680]	78.7 [3098]	83.7 [3295]
3	3 oz.	103.0 [4055]	109.6 [4315]	114.6 [4512]
4	4 oz.	137.0 [5394]	139.5 [5492]	144.5 [5689]

Reference: Min. Cu Plating Thickness
Class 1 = 20 µm [787 µin]
Class 2 = 20 µm [787 µin]
Class 3 = 25 µm [984 µin]

Table 3-12 Dielectric Withstanding Test Voltages

	Class 1	Class 2	Class 3
Voltage	No requirements	500 Vdc +15, -0	1000 Vdc +25, -0
Time	No requirements	30 sec +3, -0	30 sec +3, -0

with IPC-TM-650, Method 2.5.7. The dielectric withstanding voltage **shall** be applied between common portions of each conductor pattern and adjacent common portions of each conductor pattern. The voltage **shall** be applied between conductor patterns of each layer and the electrically isolated pattern of each adjacent layer.

3.9.2 Circuitry Flexible printed wiring **shall** be tested in accordance to IPC-9252.

3.9.2.1 Continuity Flexible printed wiring and qualification testing of flexible printed wiring **shall** be tested in accordance with the procedure outlined below. There **shall** be no circuits whose resistance exceeds the values established in the procurement documentation. The presence of long runs of very narrow conductors or high resistance metals may increase these values. When required by the user, interconnect shorts and continuity coupon D **shall** be used for evaluation of interconnection resistance and circuit continuity.

A current **shall** be passed through each conductor or group of interconnected conductors by applying electrodes on the

terminals at each end of the conductor or group of conductors. The current passing through the conductors **shall not** exceed that specified in IPC-2221 for the smallest conductor in the circuit. For qualification, the test current **shall not** exceed one ampere. Flexible printed wiring with designed resistive patterns **shall** meet the resistance requirements specified on the procurement documentation.

3.9.2.2 Isolation (Circuit Shorts) Flexible printed wiring **shall** be tested in accordance with the following procedure. The isolation resistance between conductors **shall** meet the values established in the procurement documentation.

The voltage applied between networks must be high enough to provide sufficient current resolution for the measurement. At the same time, it must be low enough to prevent arc-over between adjacent networks, which could induce defects within the product. For manual testing, the voltage **shall** be 200 volts minimum and **shall** be applied for a minimum of five seconds. When automated test equipment is used, the minimum applied test voltage **shall** be the maximum rated voltage of the flexible printed wiring up to a maximum of 40 volts.

3.9.3 Circuit/Plated-Through Hole Shorts to Metal Substrates Flexible printed wiring **shall** be tested in accordance with the procedure outlined below.

Metal core flexible printed wiring **shall** be capable of withstanding 500 volts DC between circuitry/plated-through holes and the metal core substrates. There **shall** be no flashover or dielectric breakdown.

A polarizing voltage of 500 volts DC **shall** be applied between conductors and/or lands of the flexible printed wiring and the metallic heatsink in a manner such that each conductor and/or land area is tested (e.g., using a metallic brush or aluminum foil).

3.9.4 Insulation Resistance (As Received) Test coupons **shall** be tested in accordance with IPC-TM-650, Method 2.6.3.

The insulation resistance **shall** be no less than that shown in Table 3-13. Additional insulation resistance requirements are detailed after environmental exposure to moisture (see 3.10.1).

Table 3-13 Insulation Resistance

	Class 1	Class 2	Class 3
As received	Maintain electrical function	500 MΩ	500 MΩ
After exposure to moisture	Maintain electrical function	100 MΩ	500 MΩ

3.10 Environmental Requirements When tested as specified, flexible printed wiring **shall** meet the environmental requirements detailed in 3.10.1 through 3.10.5.

3.10.1 Moisture and Insulation Resistance If required by design or procurement documentation, test coupons **shall** be tested in accordance with the procedure outlined below.

The specimen **shall not** exhibit measling, blistering, or delamination in excess of that allowed in 3.3.2. Insulation resistance **shall** meet the minimum requirements shown in Table 3-13. Noncomponent flush wiring **shall** have a minimum requirement of 50 MΩ for all classes. Moisture and insulation resistance testing for flexible printed wiring **shall** be performed in accordance with IPC-TM-650, Method 2.6.3.

3.10.2 Thermal Shock When specified on the procurement documentation, flexible printed wiring or test coupons **shall** be tested in accordance with the procedure outlined below.

The specimen **shall** be tested for thermal shock in accordance with IPC-TM-650, Method 2.6.7.2, except the temperature range **shall** be -65 °C to +125 °C [-85 °F to 257 °F]. Microsection evaluation in accordance with IPC-TM-650, Method 2.6.7.2, is not required. Following removal from the test chamber, the specimen **shall** meet the circuitry requirements of 3.9.2. The resistance value **shall not** vary by more than ± 10%.

3.10.3 Cleanliness Type 4 and Type 5 flexible printed wiring requiring permanent solder mask coating **shall** be tested and evaluated in accordance with 3.10.3.1.

3.10.3.1 Ionic (Resistivity of Solvent Extract) The specimens **shall** be tested for ionic contamination in accordance with IPC-TM-650, Method 2.3.25. When flexible printed boards are tested per this section, the contamination level **shall not** be greater than an equivalent of 1.56 µg/cm^2 of sodium chloride.

Equivalent test methods may be used in lieu of the method specified; however, it **shall** be demonstrated to have equal or better sensitivity and employ solvents with the ability to dissolve flux residue or other contaminants as does the solution presently specified.

3.10.4 Organic Contamination When specified, flexible printed wiring **shall** be tested in accordance with IPC-TM-650, Method 2.3.38 or 2.3.39. Any positive identification of organic contamination **shall** constitute a failure.

3.10.5 Fungus Resistance Completed wiring or representative wiring sections from the lot **shall not** support fungus growth when tested in accordance with IPC-TM-650, Method 2.6.1.

3.11 Special Requirements When specified on the procurement documentation, some or all of the special requirements listed in 3.11.1 through 3.11.6 **shall** apply. A special

notation on the procurement documentation will designate any special requirements.

3.11.1 Outgassing When specified, flexible printed wiring **shall** be tested in accordance with the procedure outlined below. The degree of outgassing **shall not** result in a weight loss of more than 0.1%. In lieu of testing, outgassing data from a NASA or OEM database **shall** be acceptable.

Weight loss curves **shall** be plotted on specimens of representative substrates when tested per IPC-TM-650, Method 2.6.4.

3.11.2 Impedance Testing Requirements for impedance **shall** be specified on the procurement documentation. Impedance testing may be performed on a test coupon or a designated circuit in the production wiring. Time domain reflectometers (TDR) are used for electrical testing, but for large impedance tolerances (± 10%), mechanical measurements from a microsection utilizing a special test coupon can be used.

See IPC-2251 for the equations for calculating impedance from the test coupon and the test method using the TDR technique.

3.11.3 Repair Repair of bare flexible printed boards **shall** be as agreed upon between user and supplier (see IPC-7711).

3.11.4 Circuit Repair When agreed upon between user and supplier, circuit repairs on Class 1, Class 2, and Class 3 flexible printed wiring will be permitted. As a guideline, there should be no more than two circuit repairs for each 0.09 m^2 [0.969 ft^2] or less of layer area per side. Circuit repairs on any impedance-controlled circuits **shall not** violate the impedance requirement and **shall** have the agreement of the user. Circuit repairs **shall not** violate the minimum electrical spacing requirements.

3.11.5 Rework Rework is permitted for all classes. The touch-up of surface imperfections in the base material or removal of residual plating materials or extraneous copper will be permitted for all products when such action does not affect the functional integrity of the board.

3.11.6 Coefficient of Thermal Expansion (CTE) When boards that have metal cores or reinforcements with a requirement to constrain the thermal expansion in the planar directions, the CTE **shall** be within ± 2 ppm/ °C for the CTE and temperature range specified on the master drawing. Testing **shall** be by the strain gauge method, in accordance with IPC-TM-650, Method 2.4.41.2. If agreed upon by user and supplier, other methods of determining the CTE may be used.

4 QUALITY ASSURANCE PROVISIONS

General quality assurance provisions are specified in IPC-6011 and each sectional specification. The requirements specific to flexible printed wiring are contained in this specification and include the qualification testing, sampling plan, quality performance testing and frequency, and reliability assurance inspection.

4.1 Qualification Qualification is as agreed upon by the user and supplier (see IPC-6011). The qualification shouldconsist of pre-production samples, production sample, or test specimens (see IPC-6011) that are produced by the same equipment and procedures planned for the production boards. Qualification as agreed upon by the user may consist of documentation that the supplier has furnished similar product to other users or to other similar specifications.

4.1.1 Sample Test Specimen If test specimens are used in lieu of actual production lots, the following information is provided based on previous use of standardized test specimens. Sample test specimens may be used for qualification or for ongoing process control. Master drawings, databases, or artwork phototools are available from IPC. For each type (see 1.2.2) the master drawing and artwork/phototool is listed as follows:

Type 1 Master Drawing IPC-100041,
Artwork/Phototool IPC-A-41

Type 2 Master Drawing IPC-100042,
Artwork/Phototool IPC-A-42

Type 3 Master Drawing IPC-100043,
Artwork/Phototool IPC-A-43

Type 4 Master Drawing IPC-100043,
Artwork/Phototool IPC-A-43

Type 5 Master Drawing IPC-100043,
Artwork/Phototool IPC-A-43

Note: IPC-100001 is the universal drilling and profile master drawing.

Table 4-1 specifies test coupons A through H from IPC-A-41, IPC-A-42, and IPC-A-43 to be used from the test specimen for qualification and process capability evaluations. Equivalent production board coupon descriptions can be found in IPC-2221.

Table 4-1 Qualification Testing

TEST	Requirement Paragraph	TYPE 1 & 5	TYPE 2	TYPE 3 & 4
Visual Examination	**3.3**			
Profile	3.3.1	Entire Board	Entire Board	Entire Board
Edges, Rigid Section	3.3.1.1	Entire Board	Entire Board	Entire Board
Edges, Flexible Section	3.3.1.2	Entire Board	Entire Board	Entire Board
Transition Zone, Rigid Area to Flexible Area	3.3.1.3	Entire Board	Entire Board	Entire Board
Construction Imperfections	3.3.2	Entire Board	Entire Board	Entire Board
Haloing	3.3.1.1	Entire Board	Entire Board	Entire Board
Measling	3.3.2.1	Entire Board	Entire Board	Entire Board
Crazing	3.3.2.2	Entire Board	Entire Board	Entire Board
Foreign Inclusions	3.3.2.4	Entire Board	Entire Board	Entire Board
Weave Exposure	3.3.2.5	Entire Board	Entire Board	Entire Board
Scratches, Dents, & Tool Marks	3.3.2.6	Entire Board	Entire Board	Entire Board
Surface Microvoids	3.3.2.7	Entire Board	Entire Board	Entire Board
Color Variations in Bond Enhancement Treatment	3.3.2.8	Entire Board	Entire Board	Entire Board
Pink Ring	3.3.2.9	N/A	N/A	N/A
Coverfilm Separations	3.3.2.10	Entire Board	Entire Board	Entire Board
Covercoat Requirements	3.3.2.11	Entire Board	Entire Board	Entire Board
Covercoat Coverage	3.3.2.11.1	Entire Board	Entire Board	Entire Board
Covercoat Cure & Adhesion	3.3.2.11.2	Entire Board	Entire Board	Entire Board
Covercoat Thickness	3.3.2.11.3	Entire Board	Entire Board	Entire Board
Solder Wicking/Plating Penetration	3.3.2.12	Entire Board	Entire Board	Entire Board
Stiffener	3.3.2.13	Entire Board	Entire Board	Entire Board
Plating & Coating Voids in the Hole	3.3.3	N/A	Entire Board	Entire Board
Marking	3.3.4	Entire Board	Entire Board	Entire Board
Solderability	3.3.5	A, B, A/B, C	A, B, A/B, C	A, B, A/B, C
Plating Adhesion	3.3.6	C	C	C
Edge Board Contact, Junction of Gold Plate to Solder Finish	3.3.7	Only as Required	Only as Required	Only as Required
Lifted Lands	3.3.8	Entire Board	Entire Board	Entire Board
Workmanship	3.3.9	Entire Board	Entire Board	Entire Board
Dimensional Requirements	**3.4**			
Hole Size & Hole Pattern Accuracy	3.4.1	Entire Board	Entire Board	Entire Board
Etched Annular Ring & Breakout (Internal)	3.4.2	N/A	N/A	Entire Board
Etched Annular Ring (External)	3.4.3	Entire Board	Entire Board	Entire Board
Solderable Annular Ring (External)	3.4.3.1	Entire Board	Entire Board	Entire Board
Squeeze-out of Adhesive of Coverlayer & Ooze-out of Cover Coat	3.4.3.2	Entire Board	Entire Board	Entire Board
Stiffener Access Hole	3.4.3.3	Entire Board	Entire Board	Entire Board
Bow & Twist (Individual Rigid or Stiffener Portions Only)	3.4.4	Entire Board	Entire Board	Entire Board
Conductor Definition	**3.5**			
Conductor Imperfections	3.5.1	Entire Board	Entire Board	Entire Board
Conductor Width Reduction	3.5.1.1	Entire Board	Entire Board	Entire Board
Conductor Thickness Reduction	3.5.1.2	Entire Board	Entire Board	Entire Board
Conductor Spacing	3.5.2	Entire Board	Entire Board	Entire Board

TEST	Requirement Paragraph	TYPE 1 & 5	TYPE 2	TYPE 3 & 4
Conductor Surfaces	3.5.3	Entire Board	Entire Board	Entire Board
Nicks & Pinholes in Ground or Voltage Planes	3.5.3.1	Entire Board	Entire Board	Entire Board
Surface Mount Lands	3.5.3.2	Entire Board	Entire Board	Entire Board
Edge Connector Lands	3.5.3.3	Entire Board	Entire Board	Entire Board
Dewetting	3.5.3.4	Entire Board	Entire Board	Entire Board
Nonwetting	3.5.3.5	Entire Board	Entire Board	Entire Board
Final Finish Coverage	3.5.3.6	Entire Board	Entire Board	Entire Board
Conductor Edge Outgrowth	3.5.3.7	Entire Board	Entire Board	Entire Board
Physical Requirements	**3.6**			
Bending Flexibility	3.6.1	H	H	H
Flexible Endurance	3.6.2	H	H	H
Bond Strength (Unsupported Lands)	3.6.3	A, B, or A/B	A, B, or A/B	A, B, or A/B
Bond Strength (Stiffener)	3.6.4	Only as Required	Only as Required	Only as Required
Structural Integrity	**3.7**			
Thermal Stress Testing	3.7.1	A, B, or A/B	A, B, or A/B	A, B, or A/B
Requirements for Microsectioned Coupons	3.7.2	A, B, or A/B	A, B, or A/B	A, B, or A/B
Laminate Integrity (Flexible)	3.7.3	A, B, or A/B	A, B, or A/B	A, B, or A/B
Laminate Integrity (Rigid)	3.7.4	A, B, or A/B	A, B, or A/B	A, B, or A/B
Etchback	3.7.5	N/A	N/A	A, B, or A/B
Smear Removal	3.7.6	N/A	N/A	A, B, or A/B
Negative Etchback	3.7.7	N/A	N/A	A, B, or A/B
Plating Integrity	3.7.8	N/A	A, B, or A/B	A, B, or A/B
Plating Voids	3.7.9	N/A	A, B, or A/B	A, B, or A/B
Annular Ring (Internal)	3.7.10	N/A	N/A	A, B, or A/B
Plating/Coating Thickness	3.7.11	A, B, or A/B	A, B, or A/B	A, B, or A/B
Minimum Layer Copper Foil Thickness	3.7.12	A, B, or A/B	A, B, or A/B	A, B, or A/B
Minimum Surface Conductor Thickness	3.7.13	A, B, or A/B	A, B, or A/B	A, B, or A/B
Metal Cores	3.7.14	A, B, or A/B	N/A	A, B, or A/B
Dielectric Thickness	3.7.15	A, B, or A/B	A, B, or A/B	A, B, or A/B
Resin Fill of Blind Buried Vias	3.7.16	A, B, or A/B	A, B, or A/B	A, B, or A/B
Rework Simulation	3.8	N/A	A, B, or A/B	A, B, or A/B
Electrical Requirements	**3.9**			
Dielectric Withstanding Voltage	3.9.1	E	E	E
Circuitry	3.9.2	D, H	D, H	D, H
Continuity	3.9.2.1	D, H	D, H	D, H
Isolation (Circuit Shorts)	3.9.2.2	D, H	D, H	D, H
Circuit/Plated-Through Hole Shorts to Metal Substrates	3.9.3	Only as Required	Only as Required	Only as Required
Insulation Resistance (As Received)	3.9.4	E	E	E
Environmental Requirements	**3.10**			
Moisture & Insulation Resistance	3.10.1	E	E	E
Thermal Shock	3.10.2	D	D	D
Cleanliness	3.10.3	Entire Board	Entire Board	Entire Board
Ionic (Resistivity of Solvent Extract)	3.10.3.1	Entire Board	Entire Board	Entire Board
Organic Contamination	3.10.4	Only as Required	Only as Required	Only as Required

TEST	Requirement Paragraph	TYPE 1 & 5	TYPE 2	TYPE 3 & 4
Fungus Resistance	3.10.5	Only as Required	Only as Required	Only as Required
Special Requirements	**3.11**			
Outgassing	3.11.1	Only as Required	Only as Required	Only as Required
Impedance Testing	3.11.2	Only as Required	Only as Required	Only as Required
Repair	3.11.3	Only as Required	Only as Required	Only as Required
Circuit Repair	3.11.4	Only as Required	Only as Required	Only as Required
Rework	3.11.5	Only as Required	Only as Required	Only as Required
Coefficient of Thermal Expansion (CTE)	3.11.6	Only as Required	Only as Required	Only as Required

4.2 Acceptance Testing and Frequency Acceptance testing and frequency **shall** be performed as specified in Table 4-3 to the requirements of this specification and IPC-6011 using either quality conformance coupons and/or production boards. The quality conformance test coupons are described in IPC-2221 and indicate the purpose of the coupon and its frequency on a manufacturing panel. When ''Sample'' is indicated in Table 4-3, use the C=0 Zero Acceptance Number Sampling Plan specified in Table 4-2. The C=0 Sampling Plan provides greater or equal protection for the lot tolerance percent defective (LTPD) protection at the 0.010 ''consumer risk'' level. The Index Values at the top of each sample size column associates to the AQL level. For a lot to be accepted, all samples (shown in Table 4-2) **shall** conform to the requirements. A lot is ''withheld'' if one or more samples do not conform to the requirements. A ''withheld'' lot is not considered rejected until a review by the supplier and user is completed to assess the extent and seriousness of the nonconformance. Contact the American Society for Quality Control for more information on sampling plans.

4.2.1 Referee Tests Two additional microsection sets from the same panel may be prepared and evaluated for microsection defects that are considered to be isolated, random in nature, or caused by microsection preparation. For acceptance, both referee sets must be defect free.

4.3 Quality Conformance Testing Quality Conformance Testing **shall** be performed and consist of inspections specified in Table 4-4 in a facility which meets the requirements of IPC-QL-653, unless otherwise specified by the user. Class 3 testing results may be extended to reliability test and evaluation for Class 2.

Table 4-2 C=0 Sampling Plan for Equipment Classes per Lot Size

		Class 1			Class 2			Class 3			
Lot Size	AQL	2.5	4.0	6.5	1.5	2.5	4.0	0.10	1.0	2.5	4.0
1-8		5	3	2	●	5	3	●	●	5	3
9-15		5	3	2	5	5	3	●	13	5	3
16-25		5	3	3	8	5	3	●	13	5	3
26-50		5	5	5	8	5	5	●	13	5	5
51-90		7	6	5	8	7	6	●	13	7	6
91-150		11	7	6	12	11	7	125	13	11	7
151-280		13	10	7	19	13	10	125	20	13	10
281-500		16	11	9	21	16	11	125	29	16	11
501-1.2k	501-1,200	19	15	11	27	19	15	125	34	19	15
1.2k-3.2k	1201-3,200	23	18	13	35	23	18	192	42	23	18
3.2k-10.0k	3201-10,000	29	22	15	38	29	22	294	50	29	22
10.0k-35.0k	10,001-35,000	35	29	15	46	35	29	345	60	35	29

● Denotes inspect entire lot

Table 4-3 Acceptance Testing and Frequency

Sample				Test Frequency			
Inspection	Requirement Section	Product Flexible Printed Wiring (Board)	Test Coupon by Board	Class 1[1]	Class 2[1]	Class 3[1]	Remarks
Material	3.2.1 - 3.2.12			Manufacturer's Certification			Verifiable Certificate of Compliance or SPC Program
VISUAL							
Edges, Rigid Section	3.3.1.1	X		Sample (4.0)	Sample (2.5)	Sample (2.5)	Per Board
Edges, Flex Section	3.3.1.2	X		Sample (4.0)	Sample (2.5)	Sample (2.5)	Per Board
Transition Zone, Rigid Area to Flex Area	3.3.1.3	X		Sample (4.0)	Sample (2.5)	Sample (2.5)	Per Board
Construction Imperfections	3.3.2	X		Sample (4.0)	Sample (2.5)	Sample (2.5)	Per Board
Plating and Coating Voids in Holes	3.3.3	X		Sample (4.0)	Sample (2.5)	Sample (1.0)	Per Panel Applicable to Types 2, 3 & 4 Only
Marking and Traceability	3.3.4	X	(Retained Coupons)	Sample (6.5)	Sample (4.0)	Sample (4.0)	Per Board
Edge Board Contact, Junction of Gold Plate to Solder Finish	3.3.7	X		Sample (6.5)	Sample (4.0)	Sample (2.5)	Per Panel
Lifted Lands	3.3.8	X		Sample (6.5)	Sample (4.0)	Sample (4.0)	Per Board
Workmanship	3.3.9	X		Sample (6.5)	Sample (4.0)	Sample (4.0)	Per Board
PHYSICAL							
Plating Adhesion	3.3.6	X	C	Sample (6.5)	Sample (4.0)	Sample (4.0)	Per panel (1 coupon)
Covercoat cure and adhesion	3.3.2.11.2	X	G	Sample (6.5)	Sample (4.0)	Sample (4.0)	Per panel (1 coupon)
SOLDERABILITY							
Solderability: Surface/ Hole	3.3.5		C and A or C and A/B	Sample (4.0)	Sample (2.5)	Sample (2.5)	Per Panel
DIMENSIONAL REQUIREMENTS							
Dimensional: Flexible Printed Wiring	3.4	X		Sample (6.5)	Sample (4.0)	Sample (4.0)	Per Board
Hole Size and Hole Pattern Accuracy	3.4.1	X		Sample (6.5)	Sample (4.0)	Sample (4.0)	Per Board
Etched Annular Ring and Breakout (Internal)	3.4.2		F	Not Required	Sample (1.5)	Sample (1.0)	4 Coupons Per Panel
Etched Annular Ring (External)	3.4.3	X		Sample (6.5)	Sample (4.0)	Sample (4.0)	Per Panel
Solderable Annular Ring (External)	3.4.3.1	X		Sample (6.5)	Sample (4.0)	Sample (4.0)	Per Panel
Bow and Twist (Individual Board or Stiffener Portion Only)	3.4.4	X		Sample (6.5)	Sample (4.0)	Sample (4.0)	Per Board
CONDUCTOR DEFINITION (INTERNAL AND EXTERNAL LAYERS)							
Conductor Imperfections	3.5.1	X		Sample (6.5)	Sample (4.0)	Sample (2.5)	Per Board
Conductor Width Reduction	3.5.1.1	X		Sample (6.5)	Sample (4.0)	Sample (2.5)	Per Board
Conductor Thickness Reduction	3.5.1.2	X		Sample (6.5)	Sample (4.0)	Sample (2.5)	Per Board

Sample				Test Frequency			
Inspection	Requirement Section	Product Flexible Printed Wiring (Board)	Test Coupon by Board	Class 1[1]	Class 2[1]	Class 3[1]	Remarks
CONDUCTOR DEFINITION (INTERNAL AND EXTERNAL LAYERS) – CONTINUED							
Conductor Spacing	3.5.2	X		Sample (6.5)	Sample (4.0)	Sample (2.5)	Per Board
Nicks or Pinholes in Ground or Voltage Planes	3.5.3.1	X		Sample (6.5)	Sample (4.0)	Sample (4.0)	Per Board
Surface Mount Lands	3.5.3.2	X		Sample (6.5)	Sample (4.0)	Sample (2.5)	Minimum 10 evaluations per panel
Edge Connector Lands	3.5.3.3	X		Sample (6.5)	Sample (4.0)	Sample (2.5)	Per Board
Dewetting/Nonwetting/ Final Finish Coverage	3.5.3.4 3.5.3.5 3.5.3.6	X		Sample (6.5)	Sample (4.0)	Sample (2.5)	Per Board
Conductor Edge Outgrowth	3.5.3.7	X		Sample (6.5)	Sample (4.0)	Sample (2.5)	Per Board
STRUCTURAL INTEGRITY AFTER STRESS TYPES 3-4 (MICROSECTION)							
Laminated Integrity	3.7.3 3.7.4		A or B or A/B	Sample (2.5)	Sample (1.5)	Sample (1.0)	Per panel (1 coupon)
Etchback (Type 3 and Type 4 Only)	3.7.5 3.7.6 3.7.7		A or B or A/B	Sample (2.5)	Sample (1.5)	Sample (1.0)	Per panel (1 coupon)
Plating Integrity	3.7.8		A or B or A/B	Sample (2.5)	Sample (1.5)	Sample (1.0)	Per panel (1 coupon)
Plating Voids	3.7.9		A or B or A/B	Sample (2.5)	Sample (1.5)	Sample (1.0)	Per panel (1 coupon)
Annular Ring (Internal)	3.7.10		A or B or A/B	Sample (2.5)	Sample (1.5)	Sample (1.0)	Per panel (1 coupon)
Plating/Coating Thickness	3.7.11		A or B or A/B	Sample (2.5)	Sample (1.5)	Sample (1.0)	Per panel (1 coupon)
Minimum Layer/Copper Foil Thickness	3.7.12		A or B or A/B	Sample (2.5)	Sample (1.5)	Sample (1.0)	Per panel (1 coupon)
Minimum Surface Conductor Thickness	3.7.13		A or B or A/B	Sample (2.5)	Sample (1.5)	Sample (1.0)	Per panel (1 coupon)
Metal Cores	3.7.14		A or B or A/B	Sample (2.5)	Sample (1.5)	Sample (1.0)	Per panel (1 coupon)
Dielectric Thickness	3.7.15		A or B or A/B	Sample (2.5)	Sample (1.5)	Sample (1.0)	Per panel (1 coupon)
STRUCTURAL INTEGRITY AFTER STRESS TYPE 2 (MICROSECTION)							
Laminate Integrity (Flexible)	3.7.3		A or B or A/B	Sample (6.5)	Sample (4.0)	Sample (2.5)	Per Panel
Plating Integrity	3.7.8		A or B or A/B	Sample (6.5)	Sample (4.0)	Sample (2.5)	Per Panel
Plating Voids	3.7.9		A or B or A/B	Sample (6.5)	Sample (4.0)	Sample (2.5)	Per Panel
Plating/Coating Thickness	3.7.11		A or B or A/B	Sample (6.5)	Sample (4.0)	Sample (2.5)	Per Panel
Minimum Surface Conductor Thickness	3.7.13		A or B or A/B	Sample (6.5)	Sample (4.0)	Sample (2.5)	Per Panel
Dielectric Thickness	3.7.15		A or B or A/B	Sample (6.5)	Sample (4.0)	Sample (2.5)	Per Panel
ELECTRICAL REQUIREMENTS							
Circuit Continuity	3.9.2.1	X		Sample (2.5)[2]	100%[2]	100%[2]	
Isolation (Circuit Shorts)	3.9.2.2	X		Sample (2.5)[2]	100%[2]	100%[2]	

Sample				Test Frequency			
Inspection	Requirement Section	Product Flexible Printed Wiring (Board)	Test Coupon by Board	Class 1[1]	Class 2[1]	Class 3[1]	Remarks
SPECIAL REQUIREMENTS							
Dielectric Withstand Voltage	3.9.1		Only Applicable When Imposed by Contract				
Circuits/Plated-Through Hole Shorts to Metal Substrates	3.9.3	X					
Insulation Resistance (As Received)	3.9.4						
Moisture Insulation Resistance	3.10.1						
Thermal Shock	3.10.2						
Cleanliness	3.10.3						
Ionic (Resistivity of Solvent Extract)	3.10.3.1						
Organic Contamination	3.10.4						
Fungus Resistance	3.10.5						
Dielectric Withstand Voltage	3.9.1						
Outgassing	3.11.1						
Impedance Testing	3.11.2						
Repair	3.11.3						
Circuit Repair	3.11.4						
Rework	3.11.5						
Coefficient of Thermal Expansion (CTE)	3.11.6						

NOTES:
1. Numbers in parentheses are the AQL level.
2. For Type 1 and Type 2 flexible printed wiring, visual or AOI inspection may be used in lieu of electrical testing.

Table 4-4 Quality Conformance Testing

Inspection	Requirement and Method Section	Test Coupon		Test Frequency		
		Type 1, 5	Type 2 - 4	Class 1	Class 2	Class 3
Rework Simulation	3.8		B	As required	Two coupons per QTR	Two coupons per month
Bond Strength (Unsupported Lands)	3.6.3	B	As required	As required	Two coupons per QTR	Two coupons per month
Bond Strength (Stiffener)	3.6.4	Board	Board	As required	As required	As required
Dielectric Withstanding Voltage	3.9.1	E	E	As required	Two coupons per QTR	Two coupons per month
Moisture and Insulation Resistance	3.10.1	E	E	Maintain electrical function	Two coupons per QTR	Two coupons per month

4.3.1 Coupon Selection The fabricator **shall** select two quality conformance test coupons of the most complex construction of each material slash sheet type processed during the inspection period from lots that have passed quality conformance inspection.

5 NOTES

5.1 Ordering Data The procurement documentation should specify the following:

- Title, numbers issue, revision letter, and date of current applicable procurement document.
- Specific exceptions, variations, additions, or conditions to this specification that are required by the user.
- Part identification and marking instructions.
- Information for preparation for delivery, if applicable.
- Special tests required and frequency.

5.2 Superseded Specifications This specification supersedes and replaces IPC-6013, IPC-FC-250 and IPC-RF-245.

APPENDIX A

Appendix A presents the performance requirements of IPC-6013A in an abbreviated form and alphabetical order. Special conditions, lengthy requirements, and tutorial information may be shortened or partially omitted in this appendix. See the referenced paragraph in this appendix for the full specification requirements.

Characteristic Inspection	Requirements			Requirement Paragraph
	Class 1	Class 2	Class 3	
Etched Annular Ring (External Plated-Through Holes)	Not greater than 180° breakout of hole from land when visually assessed.	Not greater than 90° breakout of hole from land when visually assessed and a 50 µm [0.0020 in] annular ring for at least 270° of the circumference.	The minimum annular ring **shall** be 50 µm [0.0020] in.	3.4.3 and Table 3-5
Etched Annular Ring (External Unsupported Holes)	Not greater than 90° breakout of hole from land when visually assessed.	Not greater than 90° breakout of hole from land when visually assessed.	The minimum annular ring **shall** be 150 µm [0.00591] in.	3.4.3 and Table 3-5
Etched Annular Ring (Internal Plated-Through Holes)	Hole breakout is allowed provided the land/ conductor junction is not reduced below the allowable width reduction in 3.5.1.1.	Hole breakout is allowed provided the land/ conductor junction is not reduced below the allowable width reduction in 3.5.1.1.	The minimum annular ring **shall** be 25 µm [0.00098 in].	3.4.2 and Table 3-5
Annular Ring (Internal)	Breakout allowed per Table 3-5.	Breakout allowed per Table 3-5.	The minimum functional internal annular ring **shall** be 25 µm [0.00098 in].	3.7.10
Bending Test	As specified in appropriate document/drawing.			3.6.1
Bond Strength (Stiffener)	Peel strength between the flexible printed wiring and the stiffener **shall** be ≥1.4 kg per 25 mm width.			3.6.4
Bond Strength (Unsupported Lands)	As per IPC-TM-650, Method 2.4.20, unsupported land **shall** withstand 1.86 kg pull or 35 kg/cm^2 [498 PSI], whichever is less, after subjection to five cycles of soldering and unsoldering.			3.6.3
Bow & Twist (Individual Rigid or Stiffener Portion Only)	Surface applications: 0.75% bow & twist (or determined by user and supplier).			3.4.4
	All other applications: 1.5% bow & twist (or determined by user and supplier).			
Characteristic Inspection for Material				3.2
Circuit Repair	No more than two repairs for each 0.09 m^2 [0.969 ft^2]; no impedance or minuimum electrical spacing req. violated.			3.11.4
Circuitry	Testing conducted in accordance with IPC-9252.			3.9.2
Circuits/Plated-Through Hole Shorts to Metal Substrates	Metal core flexible printed board **shall** withstand 500 volts DC between circuitry/ plated-through holes and metal core substrates w/o flashover or dielectric breakdown.			3.9.3
Cleanliness	Type 4 & Type 5 flexibles **shall** be tested and evaluated in accordance with 3.10.3.1.			3.10.3
Coefficient of Thermal Expansion	If have metal cores/reinforcements with a req. to constrain thermal expansion in planar directions, CTE **shall** be within ± 2 ppm/ °C for CTE & temp range spec on master drawing; testing w/ strain gauge method, according to IPC-TM-650, Method 2.4.41.2 unless otherwise agreed by user and supplier.			3.11.6
Color Variations in Bond Enhancement Treatment	Mottled appearance/color variation accept; Random missing areas of treatment **shall not** be >10%.			3.3.2.8
Conductor Definition	Meet visual & dimension req., pattern & thickness as specified in procurement documentation.			3.5
Conductor Edge Outgrowth	No outgrowth on edges of conductors that have been solder coated or electrodeposited tin-lead plated and fused when tested according to IPC-TM-650, Method 2.4.1.			3.5.3.7

Characteristic Inspection	Requirements			Requirement Paragraph
	Class 1	Class 2	Class 3	
Conductor Imperfections	Cross-sectional area of conductor not reduced >30% of minimum value.	Cross-sectional area of conductor not reduced >20% of minimum value; total defect not >10% of conductor or 13 mm (whichever is less).		3.5.1
	No cracks, splits or tears.			
Conductor Spacing	Minimum conductor spacing may be reduced an additional 30% due to conductor edge roughness, spikes, etc.		Minimum conductor spacing may be reduced an additional 20% due to conductor roughness, spikes, etc.	3.5.2
Conductor Surfaces				3.5.3
Conductor Thickness Reduction	Reduction of conductor thickness not >30% of minimum.	Reduction of conductor thickness not >20% of minimum.		3.5.1.2
Conductor Width Reduction	Reduction of conductor width not >30% of minimum	Reduction of conductor width not >20% of minimum.		3.5.1.1
Construction Imperfections	Measling, crazing, blistering and delamination.			3.3.2
Continuity	No circuits with resistance > the values established in the procurement documentation; current passed through for evaluation will not be > values in IPC-2221 for smallest conductor of circuit.			3.9.2.1
Covercoat Coverage	Conductors not exposed where covercoat required.			3.3.2.11.1
	Blistering does not bridge between conductors.	Two per side, max size 0.25 mm [0.00984 in] in longest dim, spacing between conductors not reduced by more than 25%.		
Covercoat Cure and Adhesion	Max % loss allowed: Bare Copper - 10 Gold or Nickel - 25 Base Laminate - 10 Melting Metals - 50	Max % loss allowed: Bare Copper - 5 Gold or Nickel - 10 Base Laminate - 5 Melting Metals - 25	Max % loss allowed: Bare Copper - 0 Gold or Nickel - 5 Base Laminate - 0 Melting Metals -10	3.3.2.11.2
Covercoat Requirements	See 3.3.2.11.1 through 3.3.2.11.3.			3.3.2.11
Covercoat Thickness	Not measured unless required by procurement documentation.			3.3.2.11.3
Coverfilm Separations	Uniform coverfilm, free of separations. Nonlamination good if according to 3.3.2.4, not >0.80 mm x 0.80 mm [0.0315 in x 0.0315 in], not >3 in 25 mm x 25 mm [0.984 in x 0.094 in] space, not >25% of spacing between conductors.			3.3.2.10
Crazing	Imperfection does not reduce the conductor spacing below the minimum and there is no propagation of the imperfection as a result of thermal testing that replicates the manufacturing process. For Class 2 and 3, the distance of crazing **shall not** span more than 50% of the distance between adjacent conductors.			3.3.2.2
Delamination/Blistering	Acceptable for all classes of end product provided the area affected by imperfections does not exceed 1% of the board area on each side and does not reduce the spacing between conductive patterns below the minimum conductor spacing. There **shall** be no propagation of imperfections as a result of thermal testing that replicates the manufacturing process. For Class 2 and 3, the blister or delamination **shall not** span more than 25% of the distance between adjacent conductive patterns.			3.3.2.3
Dewetting	Solder connection: 15%	Solder connection: 5%		3.5.3.4
	Conductors and planes are permitted.			
Dielectric Thickness	The minimum dielectric spacing **shall** be specified on the procurement documentation.			3.7.15
Dielectric Withstand Voltage	See Table 3-12; the dielectric withstanding voltage test **shall** be performed in accordance with IPC-TM-650, Method 2.5.7.			3.9.1
Dimensional Requirements	As specified in procurement documentation.			3.4
Edge Board Contact, Junction of Gold Plate to Solder Finish	Copper: 2.5 mm [0.0984 in]	Copper: 1.25 mm [0.04291 in]	Copper: 0.8 mm [0.031 in]	3.3.7
	Gold: 2.5 mm [0.0984 in]	Gold: 1.25 mm [0.04291 in]	Gold: 0.8 mm [0.031 in]	

Characteristic Inspection	Requirements			Requirement Paragraph
	Class 1	Class 2	Class 3	
Edge Connector Lands	No cuts or scratches that expose nickel or copper; Pits, dents, or depressions accept if not exceed 0.15 mm [0.00591 in] in longest dimension with no more than 3 per land, and not appear in >30% of lands.			3.5.3.3
Edges, Flexible Section	Free of burrs, nicks, or delamination in excess of that allowed in the procurement documentation (except if a result of tie-in tabs to facilitate circuit removal). Tears **shall not** be allowed in Type 1 or Type 2 flexible printed wiring.			3.3.1.2
Edges, Ridged Section	Accept if penetration not >50% of distance from edge to nearest conductor or 2.5 mm [0.0984 in], whichever is less.			3.3.1.1
Electrical	Voltage: No requirements	Voltage: 500Vdc (+15, -0)	Voltage: 1000 Vdc (+25, -0)	3.9
	Time: No requirements	Time: 30 sec (+3, -0)	Time: 30 sec (+3, -0)	
Environmental				3.10
Etchback (Type 3 & Type 4 Only)	Between 0.003 mm [0.000118 in] (copper exposed) and 0.08 mm [0.00315 in] (maximum material removed).			3.7.5
Final Finish Coverage	Exposed copper on area not to be soldered allowed up to 5%.			3.5.3.6
	Shall meet requirements of J-STD-003.			
Flexible Endurance	As specified in appropriate document/drawing, according to IPC-TM-650, Method 2.4.3.			3.6.2
Foreign Inclusions	Translucent particles trapped within the board **shall** be acceptable. Other particles trapped within the board **shall** be acceptable provided the particle does not reduce the spacing between adjacent conductors to below the minimum spacing specified in 3.5.2.			3.3.2.4
Fungus Resistance	No fungus growth when tested in accordance with IPC-TM-650, Method 2.6.1.			3.10.5
Haloing	Does not penetrate more than 2.5 mm [0.0984 in] or 50% of distance to closest conductor, whichever is less.			3.3.1.1
Hole Size and Hole Pattern Accuracy	As specified in procurement documentation.			3.4.1
Impedance Testing	As specified in procurement documentation; TDR used for electrical testing, but for large impedance tolerances (± 10%), mechanical measurements from a microsection utilizing a special test coupon.			3.11.2
Insulation Resistance (As Received)	As received: Maintain electrical function	As received: 500 megohms		3.9.4
	After exposure to moisture: Maintain electrical function	After exposure to moisture: 100 megohms	After exposure to moisture: 500 megohms	
Ionic (Resistivity of Solvent Extract)	Testing in accordance to IPC-TM-650, Method 2.3.25, with contamination level of >1.56 µg/cm^2 of sodium chloride.			3.10.3.1
Isolation (Circuit Shorts)	Isolation resistance between conductors **shall** meet values established in the procurement documentation; 200 volt minimum for manual testing for at least five seconds; for automated tests, if mininum voltage not specified, use up to a maximum of 40 volts.			3.9.2.2
Laminate Integrity (Flexible)	No laminate voids in Zone B (see Figure 3-12) in excess of 0.50 mm [0.0197 in].			3.7.3
Laminate Integrity (Rigid)	See section 3.7.4 and Figure 3-12.			3.7.4
Lifted Lands	No lifted lands.			3.3.8
Marking	Conductive marking must be compatible with materials, and not reduce electrical spacing requirements.			3.3.4
Material	Manufacturer's Certification.			
Measling	Measling **shall** be acceptable except for high-voltage applications.			3.3.2.1
Metal Cores	Wicking, radial cracks, lateral spacing, or voids in the hole-fill insulation material **shall not** reduce electrical spacing between adjacent conductive surfaces to <0.100 mm [0.00394 in].			3.7.14
Minimum Layer/Copper Foil Thickness	If not specified in procurement documentation, see Table 3-10.			3.7.12
Minimum Surface Conductor Thickness	If not specified in procurement documentation, see Table 3-11.			3.7.13

Characteristic Inspection	Requirements			Requirement Paragraph
	Class 1	Class 2	Class 3	
Moisture and Insulation Resistance	No measling, blistering or delamination in excess of that allowed in 3.3.2; insulation resistance meet requirements of Table 3-13; moisture & insulation resistance testing according to IPC-TM-650.			3.10.1
Negative Etchback	Not to exceed 25 µm [984 µin] if etchback not specified on procurement documentation.	Not to exceed 25 µm [984 µin] if etchback not specified on procurement documentation.	Not to exceed 13 µm [512 µin] if etchback not specified on procurement documentation.	3.7.7
Nicks and Pinholes in Ground or Voltage Planes	Maximum size 1.5 mm [0.0591 in].	Maximum size 1.0 mm [0.0394 in].		3.5.3.1
Nonwetting	For tin, tin/lead reflowed, or solder coated surfaces, only allowed outside minimum solderable area or annular ring requirement.			3.5.3.5
Organic Contamination	Tested according to IPC-TM-650, Method 2.3.38 or 2.3.39, with no positive id of organic contamination.			3.10.4
Outgassing	Testing in accordance to procurement documentation; not resulting in a weight loss of more than 0.1%.			3.11.1
Physical Requirements				3.6
Pink Ring	Acceptable.			3.3.2.9
Plating Adhesion	No portion of protective plating or conductor pattern foil **shall** be removed. Testing in accordance with IPC-TM-650, Method 2.4.1.			3.3.6
Plating/Coating Thickness	**Shall** meet requirements of Table 1-1 or as specified in procurement documentation, isolated areas of reduced copper thickness **shall** be measured and evaluated to the copper plating void rejection criteria specified in 3.3.3.			3.7.11
Plating and Coating Voids in the Hole	Copper: 3 voids per hole in ≤10% of holes.	Copper: 1 void per hole in ≤5% of holes.	Copper: none	3.3.3
	Finish Coating: 5 voids per hole in ≤15% of holes.	Finish Coating: 3 voids per hole in ≤5% of holes.	Finished Coating: 1 void per hole in ≤5% of holes.	
Plating Integrity		No separation of layers (except as noted in Table 3-9).		3.7.8
	Areas of contamination or inclusions not to exceed 50% of each side of the interconnection or occur in the interface of the copper cladding on the core and the copper plating in the hole wall.			
Plating Voids	Meet requirements established in Table 3-9.	No more than 1 void per specimen, regardless of length or size. No plating void in excess of 5% of total flex PCB thickness. No plating voids evident at internal layer and PTH hole wall interface.		3.7.9
Repair	As agreed upon by user and supplier.			3.11.3
Requirements for Microsectioned Coupons	See Table 3-9 and 3.7.3 through 3.7.16.			3.7.2
Resin Fill of Blind and Buried Vias	No fill requirement.			3.7.16
Rework	Does not affect functional integrity of board.			3.11.5
Scratches, Dents, and Tool Marks	Not bridge conductors, expose fibers > allowed in 3.3.2.4 and 3.3.2.5, and do not reduce dielectric spacing below minimum.			3.3.2.6
Smear Removal (Type 3 & Type 4 Only)	**Shall** be sufficient to completely remove resin from surface of the conductor interface (see Figure 3-14).			3.7.6
Solder Wicking/Plating Migration	As agreed upon between user and supplier	0.5 mm [0.020 in] maximum.	0.3 mm [0.012 in] maximum.	3.3.2.12
Solderability	Solderability testing and accelerated aging will be in accordance to J-STD-003.			3.3.5
Solderable Annular Ring (External)	Meet requirements of Table 3-7.			3.4.3.1
Special	As specified in procurement documentation.			3.11
Stiffener	Requirements agreed upon between user and supplier.			3.3.2.13

Characteristic Inspection	Requirements			Requirement Paragraph
	Class 1	Class 2	Class 3	
Stiffener Access Hole	**Shall not** reduce external annular ring requirements below that specified in 3.4.3.			3.4.3.3
Structural Integrity	**Shall** meet structural integrity requirements for thermally stressed (after solder float) evaluation coupons specified in 3.7.2.			3.7
Surface Microvoids	Not exceed 0.8 mm [0.0315 in] in longest dimension, bridge conductors, nor exceed 5% of printed area.			3.3.2.7
Surface Mount Lands	Defects along edge of land not >30%; internal defects not >20%.	Defects along edge of land not >20%; internal defects not >10%.		3.5.3.2
Thermal Shock	Testing/evaluation according to IPC-TM-650, Method 2.6.7.2, with temp range between -65 °C to 125 °C [-85 °F to 257 °F].			3.10.2
Thermal Stress Testing	Specimens conditioned by baking at 120 °C to 150 °C [248 °F to 302 °F] for six hours, depending on thickness and according to IPC-TM-650, Method 2.6.8. After microsectioning, plated-through holes **shall** be examined for foil and plating at 100X ± 5%. Referee examinations made at 200X (± 5%).			3.7.1
Transition Zone, Rigid Area to Flexible Area	Imperfections in excess of that allowed **shall** be agreed upon between the fabricator and user, or as so stated on the procurement documentation.			3.3.1.3
Visual	Finished product **shall** be examined, be of uniform quality, and conform to 3.3.1 through 3.3.9.			3.3
Weave Exposure	Acceptable if does not reduce conductor spacing below minimum.			3.3.2.5
Workmanship	**Shall** be free of defects and of uniform quality - no visual of dirt, foreign matter, oil, fingerprints.			3.3.9

IPC
ASSOCIATION CONNECTING
ELECTRONICS INDUSTRIES®

ANSI/IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits Definition Submission/Approval Sheet

The purpose of this form is to keep current with terms routinely used in the industry and their definitions. Individuals or companies are invited to comment. Please complete this form and return to:

IPC
2215 Sanders Road
Northbrook, IL 60062-6135
Fax: 847 509.9798

SUBMITTOR INFORMATION:

Name: _____

Company: _____

City: _____

State/Zip: _____

Telephone: _____

Date: _____

❑ This is a **NEW** term and definition being submitted.
❑ This is an **ADDITION** to an existing term and definition(s).
❑ This is a **CHANGE** to an existing definition.

Term	Definition

If space not adequate, use reverse side or attach additional sheet(s).

Artwork: ❑ Not Applicable ❑ Required ❑ To be supplied
❑ Included: Electronic File Name: _____

Document(s) to which this term applies: _____

Committees affected by this term: _____

Office Use

IPC Office	Committee 2-30
Date Received: _____	Date of Initial Review: _____
Comments Collated: _____	Comment Resolution: _____
Returned for Action: _____	Committee Action: ❑ Accepted ❑ Rejected
Revision Inclusion: _____	❑ Accept Modify

IEC Classification

Classification Code • Serial Number

Terms and Definition Committee Final Approval Authorization:
Committee 2-30 has approved the above term for release in the next revision.

Name: _____ Committee: IPC 2-30 Date: _____

Technical Questions

The IPC staff will research your technical question and attempt to find an appropriate specification interpretation or technical response. Please send your technical query to the technical department via:

tel 847/509-9700 fax 847/509-9798
www.ipc.org e-mail: answers@ipc.org

IPC World Wide Web Page www.ipc.org

Our home page provides access to information about upcoming events, publications and videos, membership, and industry activities and services. Visit soon and often.

IPC Technical Forums

IPC technical forums are opportunities to network on the Internet. It's the best way to get the help you need today! Over 2,500 people are already taking advantage of the excellent peer networking available through e-mail forums provided by IPC. Members use them to get timely, relevant answers to their technical questions. Contact KeachSasamori@ipc.org for details. Here are a few of the forums offered.

TechNet@ipc.org

TechNet forum is for discussion of issues related to printed circuit board design, assembly, manufacturing, comments or questions on IPC specifications, or other technical inquiries. IPC also uses TechNet to announce meetings, important technical issues, surveys, etc.

ComplianceNet@ipc.org

ComplianceNet forum covers environmental, safety and related regulations or issues.

DesignerCouncil@ipc.org

Designers Council forum covers information on upcoming IPC Designers Council activities as well as information, comments, and feedback on current designer issues, local chapter meetings, new chapters forming, and job opportunities. In addition, IPC can set up a mailing list for your individual Chapter so that your chapter can share information about upcoming meetings, events and issues related specifically to your chapter.

Gencam@ipc.org

Gencam deals with issues regarding the Gencam™ standards and specifications for Printed Circuit Board Layout and Design.

LeadFree@ipc.org

This forum acts as a peer interaction resource for staying on top of lead elimination activities worldwide and within IPC.

IPC_New_Releases@ipc.org

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ADMINISTERING YOUR SUBSCRIPTION STATUS:

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The associated e-mail message text will be distributed to everyone on the list, including the sender. Further information on how to access previous messages sent to the forums will be provided upon subscribing.

For more information, contact Keach Sasamori
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e-mail: sasako@ipc.org www.ipc.org/html/forum.htm

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IPC Printed Circuits Expo is the largest trade exhibition in North America devoted to the PWB manufacturing industry. Over 90 technical presentations make up this superior technical conference. Visit www.ipcprintedcircuitexpo.org for upcoming dates and information.

Exhibitor information:
Contact: Mary MacKinnon
Sales Manager
tel 847/790-5386
e-mail: MaryMackinnon@ipc.org

Alicia Balonek
Exhibits Manager
tel 847/790-5398
e-mail: AliciaBalonek@ipc.org

Registration information:
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APEX is the premier technical conference and exhibition dedicated entirely to the electronics assembly industry. Visit www.GoAPEX.org for upcoming dates and more information.

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e-mail: MaryMacKinnon@ipc.org

Registration information:
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fax 847/509-9798
e-mail: goapex@ipc.org

How to Get Involved

The first step is to join IPC. An application for membership can be found in the back of this publication. Once you become a member, the opportunities to enhance your competitiveness are vast. Join a technical committee and learn from our industry's best while you help develop the standards for our industry. Participate in market research programs which forecast the future of our industry. Participate in Capitol Hill Day and lobby your Congressmen and Senators for better industry support. Pick from a wide variety of educational opportunities: workshops, tutorials, and conferences. More up-to-date details on IPC opportunities can be found on our web page: www.ipc.org.

For information on how to get involved, contact:
Jeanette Ferdman, Membership Director
tel 847/790-5309 fax 847/509-9798
e-mail: JeanetteFerdman@ipc.org www.ipc.org

Application for IPC Site Membership

IPC
ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES®

Thank you for your decision to join IPC, Association Connecting Electronics Industries. IPC membership is site specific, which means that benefits of IPC membership are extended only to employees at the site that is designated on this application.

To help IPC serve your member site in the most effective manner possible, please tell us what work is being done at your site by choosing the most appropriate member category. *(Check one box only.)*

❑ INDEPENDENT PRINTED CIRCUIT BOARD MANUFACTURER

This facility manufactures, and sells to other companies, printed wiring boards (PWB's) or other electronic interconnection products on the merchant market.

What products do you make for sale?

❑ One- and two-sided rigid, multilayer printed boards ❑ Flexible printed boards ❑ Other interconnections

Site General Manager_____
Name Title

❑ EMSI COMPANY - Independent Electronics Assembly

This facility assembles printed wiring boards, on a contract basis, and may offer other electronic interconnection products for sale.

Site General Manager_____
Name Title

❑ OEM - Original Equipment Manufacturer

This facility purchases and/or manufactures printed wiring boards or other interconnection products for use in a final product, which we manufacture and sell.

What is your company's primary product line?

_____

Site General Manager _____
Name Title

❑ INDUSTRY SUPPLIER

This facility supplies raw materials, machinery, equipment, or services used in the manufacture or assembly of electronic interconnection products.

What products or services does your company supply? (50 word limit, please)
The information that you provide here will appear in the next edition of the IPC Membership Directory.

Our company supplies:

_____

_____

_____

_____

❑ GOVERNMENT AGENCY/ACADEMIC TECHNICAL LIAISON

This government agency or accredited university, college or technical training school is directly concerned with design, research and utilization of electronic interconnection devices. (Must be a non-profit or not-for-profit organization.)

Please proceed to page 2 to complete the membership application.

Application for IPC Site Membership

IPC
ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES®

Site Information: (Please print or type)

Company Name

Street Address

City	State	Zip/Postal Code	Country

Main Switchboard Phone No	Main Fax No.
Company E-Mail Address	Website URL
Name of Primary Contact for all IPC matters	Title	Mail Stop
Phone No.	Fax No	E-Mail
Name of Senior Management Contact:	Title:	Mail Stop
Phone No	Fax No	E-Mail

Please attach business card of primary contact here.

Please designate your site's Technical Representatives:

For PWB/PWA design-related information and activities:

Contact Name	Title	Phone	Fax	E-mail

For PCB fabrication-related information and activities:

Contact Name	Title	Phone	Fax	E-mail

For Electronics Assembly-related information and activities:

Contact Name	Title	Phone	Fax	E-mail

Please designate your site's Management Representatives:

For PWB/PWA design-related information and activities:

Contact Name	Title	Phone	Fax	E-mail

For PCB fabrication-related information and activities:

Contact Name	Title	Phone	Fax	E-mail

For Electronics Assembly-related information and activities:

Contact Name	Title	Phone	Fax	E-mail

Please proceed to page 3 to complete the membership application.

Application for IPC Site Membership

IPC
ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES®

MEMBERSHIP DUES SCHEDULE

Please check one:

- ❑ **$1,000.00 –** Annual dues for Primary Site Membership
  Twelve months of IPC membership begins from the time the application and payment are received at the IPC office.
- ❑ **$800.00 –** Annual dues for Additional Facility Membership
  An additional membership for a site within an organization where there already is a current Primary Site IPC membership.
- ❑ **$600.00** –** Annual dues for an independent PCB/PWA fabricator or independent EMSI provider with annual sales of less than $1,000,000.00. USD
  ** Please provide proof of annual sales.
- ❑ **$250.00 –** Annual dues for Government Agency or Academic Technical Liaison Membership. Must be not-for-profit organization.

TMRC MEMBERSHIP

- ❑ Please send information on participation in the Technology Market Research Council (TMRC) program. Only current IPC member sites are eligible to participate in this **calendar year** program, which is available for an additional fee.
- ❑ **Yes, sign up our site now:**
  $950.00 - Primary TMRC member site
  $400.00 - Additional facility TMRC member. Another site within our organization is already a TMRC program participant.

Name of Primary Contact for all TMRC matters:

_____

_____
Phone Fax

_____
E-Mail

PAYMENT INFORMATION

Enclosed is our check/money order for $_____

Mail application with check or money order to:

IPC
Dept. 77-3491
Chicago, IL 60678-3491

Fax or mail application with credit card payment to:

IPC
***2215 Sanders Road**
Northbrook, IL 60062-6135
Tel: 847-509-9700
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Please bill my credit card (circle one) for $_____

❑ MasterCard ❑ American Express ❑ Visa ❑ Diners Club

_____
Account No Expiration Date

_____
Name of Card Holder

_____
Authorized Signature

_____
Phone Number

QUESTIONS?

Call the IPC Member Services Department in Northbrook, Illinois, at: 847-509-9700 (extensions 5309/5372)

or fax us at 847.509-9798

E-mail: JeanetteFerdman@ipc.org SusanStorck@ipc.org

Please proceed to page 4 to complete the membership application.

Application for IPC Site Membership

INFORMATION DISTRIBUTION

IPC has significant member benefits available to a wide range of individuals within your organization. To ensure that your facility takes advantage of these benefits, please provide the name of the individual responsible for each of the functional areas listed below. If one person has multiple responsibilities, please list that person's name as many times as necessary.

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Name | Title/Mail Stop | Phone | Fax | E-mail

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Name | Title/Mail Stop | Phone | Fax | E-mail

Finance (CFO)

Name | Title/Mail Stop | Phone | Fax | E-mail

Human Resources

Name | Title/Mail Stop | Phone | Fax | E-mail

Environmental/Safety

Name | Title/Mail Stop | Phone | Fax | E-mail

Design/Artwork

Name | Title/Mail Stop | Phone | Fax | E-mail

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Name | Title/Mail Stop | Phone | Fax | E-mail

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Name | Title/Mail Stop | Phone | Fax | E-mail

Training

Name | Title/Mail Stop | Phone | Fax | E-mail

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Name | Title/Mail Stop

Name | Title/Mail Stop

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Name | Title/Mail Stop

Name | Title/Mail Stop

ASSOCIATION CONNECTING
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Standard Improvement Form

IPC-6013A

The purpose of this form is to provide the Technical Committee of IPC with input from the industry regarding usage of the subject standard.

Individuals or companies are invited to submit comments to IPC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

IPC
2215 Sanders Road
Northbrook, IL 60062-6135
Fax 847 509.9798
E-mail: answers@ipc.org

1. I recommend changes to the following:

___ Requirement, paragraph number _____

___ Test Method number _____, paragraph number _____

The referenced paragraph number has proven to be:

___ Unclear ___ Too Rigid ___ In Error

___ Other _____

2. Recommendations for correction:

_____

_____

_____

_____

3. Other suggestions for document improvement:

_____

_____

_____

_____

Submitted by:

Name _____ Telephone _____

Company _____ E-mail _____

Address _____

City/State/Zip _____ Date _____

ASSOCIATION CONNECTING
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